VS-702

Voltage Controlled SAW Oscillator
Previous Vectron Model VS-720

Description

The VS-702 is a SAW Based Voltage Controlled Oscillator that achieves low phase noise and very low jitter performance. The VS-702 is housed in an industry standard hermetically sealed LCC package and available in tape and reel.

Features

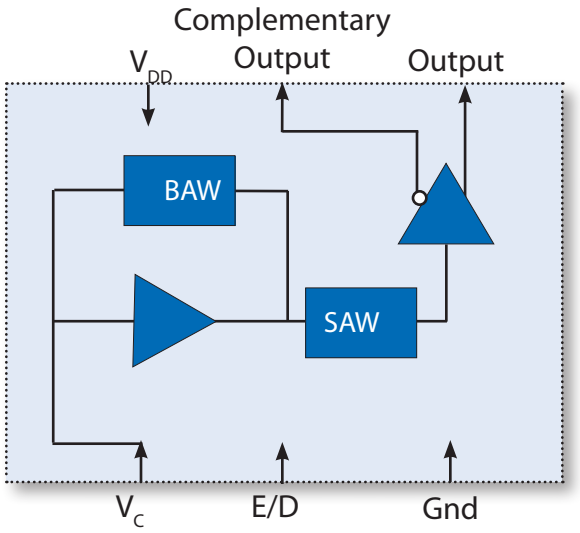
- Industry Standard Package, 5.0 x 7.5 x 2.0 mm
- ASIC Technology for Ultra Low Jitter
  0.100 ps-rms typical across 12 kHz to 20 MHz BW
  0.120 ps-rms typical across 50 kHz to 80 MHz BW
- Output Frequencies from 150 MHz to 1 GHz
- 3.3 V Operation
- LV-PECL or LVDS Configuration with Fast Transition Times
- Improved Temperature Stability over Standard VCSO (±20 ppm)
- Output Disable Feature
- 0/70°C or -40/85°C operating temperature
- Product is free of lead and compliant to EC RoHS Directive

Applications

Ideal for PLL circuits for clock smoothing and frequency translation

- SONET, SDH
- Synchronous Ethernet
- Fiber Channel
- LAN / WAN
- Test and Measurement

Block Diagram

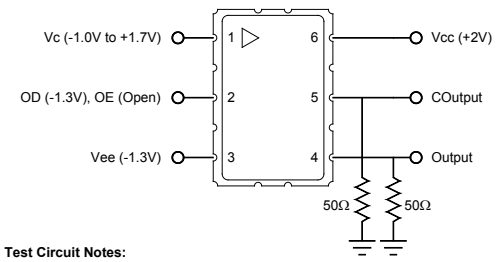


Performance Specifications

Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	2.97	3.3	3.63	V
Current (No Load)	I_{DD}		70	90	mA
Frequency					
Nominal Frequency[2]	f_N	150		1000	MHz
Absolute Pull Range [3,6]	APR	±50			ppm
Linearity[3]	Lin		5	10	%
Gain Transfer Positive[3] (See pg 3)	K_V		+100		ppm/V
Temperature Stability[3]	f_{STAB}		±20		ppm
Outputs					
Mid Level[3]		V_{DD}-1.5	V_{DD}-1.3	V_{DD}-1.2	V
Single Ended Swing[3]			750		mV-pp
Double Ended Swing[3]			1.5		V-pp
Current	I_{OUT}			20	mA
Rise/Fall Time[4]	t_R/t_f			500	ps
Symmetry[3]	SYM	45	50	55	%
Jitter (12 kHz - 20 MHz BW)622.08MHz[5]	ϕJ		0.1	0.25	ps-rms
Jitter (50 kHz - 80 MHz BW)155.52MHz[5]	ϕJ		0.12	0.30	ps-rms
Period Jitter, RMS (622.08MHz)[7]	ϕJ		2.5	3.0	ps
Period Jitter, Peak - Peak (622.08MHz)[7]	ϕJ		16	24	ps
Spurious Suppression[2]			-60	-50	dBc
Control Voltage					
Control Voltage Range for APR	V_C	0.3		3.0	V
Control Voltage Input Impedance	Z_{IN}	75			KΩ
Control Voltage Modulation BW	BW	50			kHz
Enable/Disable					
Output Enabled, Option A Output Disabled, Option A	V_{IH} V_{IL}	0.7*V_{DD}		 0.3*V_{DD}	V V
Output Enabled, Option C Output Disabled, Option C	V_{IL} V_{IH}	 0.7*V_{DD}		0.3*V_{DD}	
Operating Temperature	T_{OP}	0/70 or -40/85			°C
Package Size		5.0 x 7.5 x 2.0			mm

1] The VS-702 power supply should be filtered, eg, 0.1 and 0.01uF to ground
2] See Standard Frequencies and Ordering Information tables for more specific information
3] Parameters are tested with production test circuit below (Fig 1).
4] Measured from 20% to 80% of a full output swing (Fig 2).
5] Integrated across stated bandwidth.
6] Tested with Vc = 0.3V to 3.0V unless otherwise stated in part description
7] Broadband Period Jitter measured using Lecroy Wavemaster 8600A 6 GHz Oscilloscope, 25K samples taken. See application note.



Test Circuit Notes:
1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased Down 1.3V.
2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.
3) 50Ω Terminations are Within Test Equipment.

Fig 1: Test Circuit

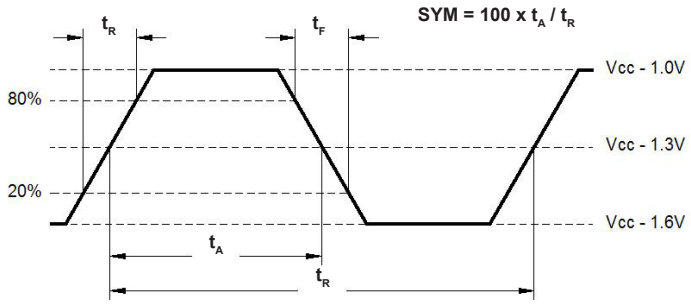
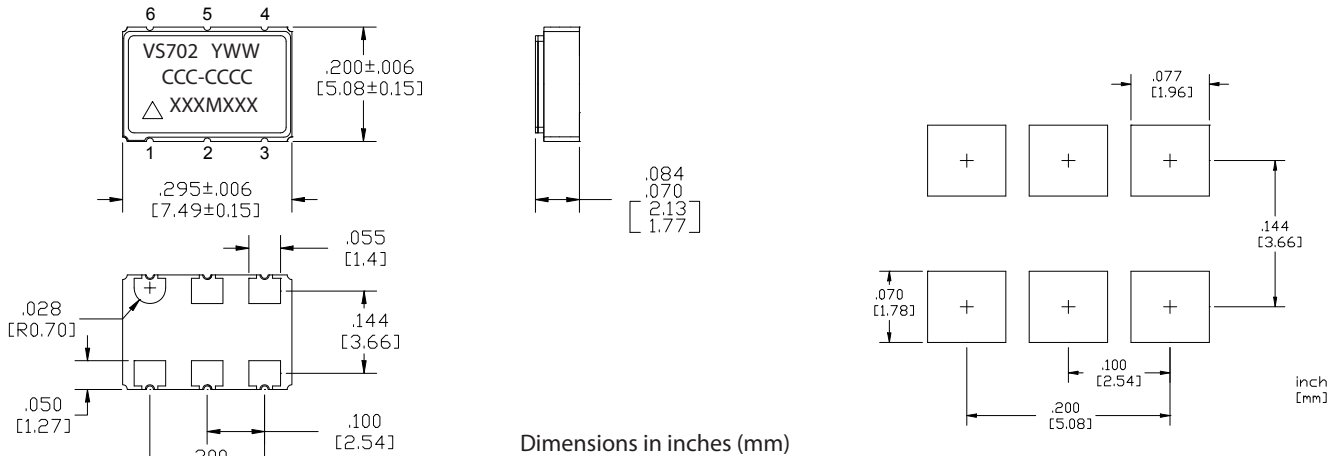


Fig 2: LVPECL Waveform

Outline Drawing & Pad Layout

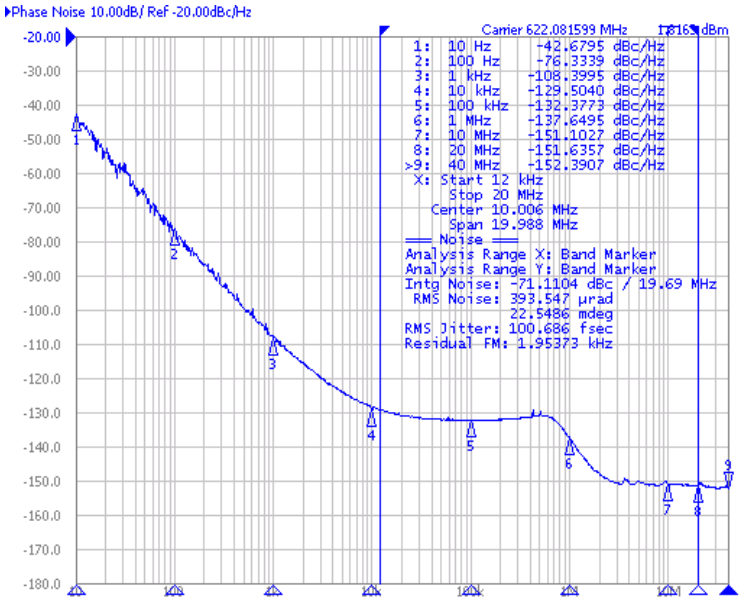


Dimensions in inches (mm)

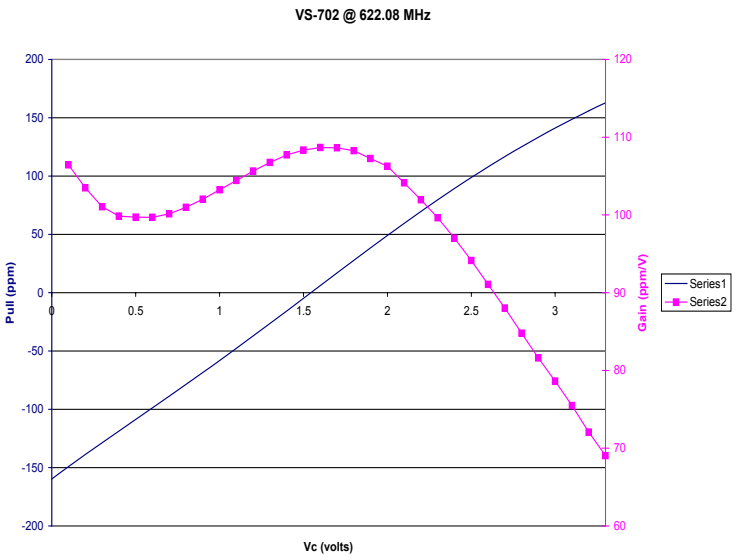
Table 2. Pin Out

Pin	Symbol	Function
1	V_C	VCXO Control Voltage
2	OE	Enable/Disable **See Ordering Options**
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	V_{DD}	Power Supply Voltage (3.3V ±10%)

Typical Phase Noise



Typical Gain



Suggested Output Load Configurations

The VS-702 incorporates a standard PECL output scheme, which are un-terminated emitters as shown in Figure 3. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 4, and a pull-up/pull-down scheme as shown in Figure 5. An AC coupling capacitor is optional, depending on the application and the input logic requirements of the next stage.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

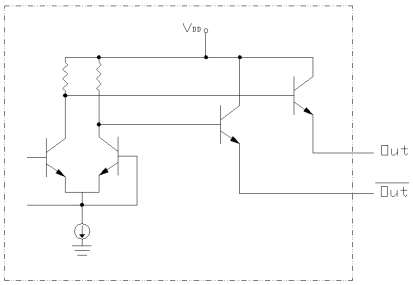


Figure 3 Standard PECL Output Configuration

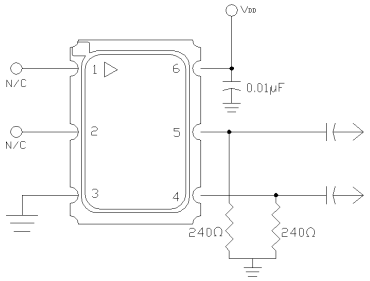


Figure 4 Single Resistor Termination Scheme
Resistor values are typically 120 to 240 ohms

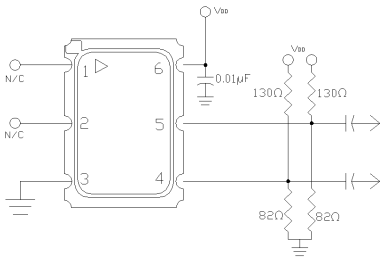


Figure 5 Pull-Up Pull-Down Termination

Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VS-702 family is capable of meeting the following qualification tests:

Table 3. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold over Nickel

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if OD or Vc is applied before Vcc.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	0 to 6	V
Output Current	I_{OUT}	25	mA
Voltage Control Range	V_C	0 to V_{DD}	V
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	T_{LS}	260 / 40	°C / sec

Although ESD protection circuitry has been designed into the VS-702 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

Table 5. ESD Ratings

Model	Minimum	Conditions
Human Body Model	500V	MIL-STD-883, Method 3015
Charged Device Model	500V	JESD22-C101

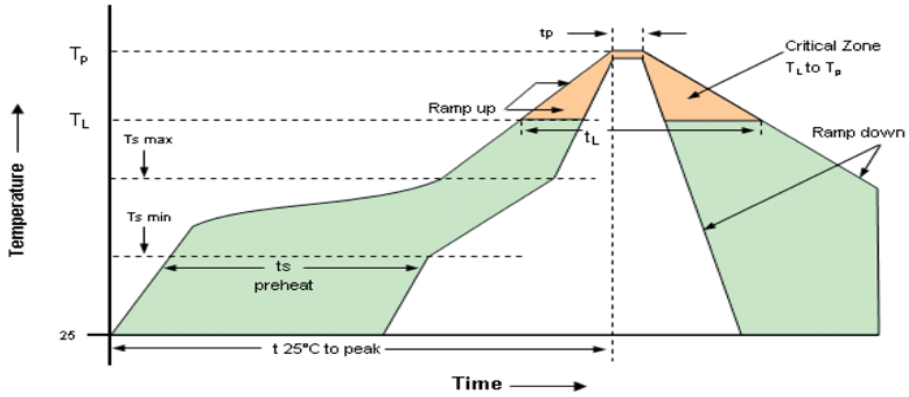
IR Reflow

Table 6. Reflow Profile (IPC/JEDEC J-STD-020C)		
Parameter	**Symbol**	**Value**
PreHeat Time Ts-min Ts-max	t_S	60 sec Min, 180 sec Max 150°C 200°C
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	$T_{25C\ to\ peak}$	480 sec Max
Time at 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

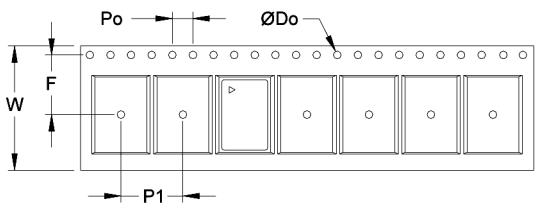
The device is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VS-702 device is hermetically sealed so an aqueous wash is not an issue.

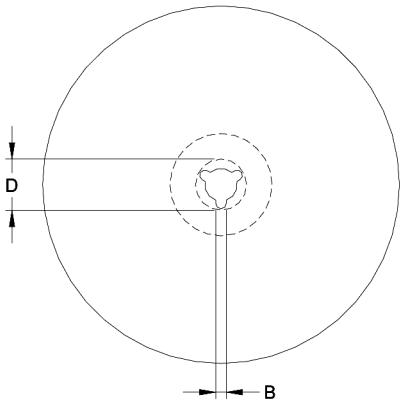
Termination Plating:
Electroless Gold Plate over Nickel Plate

Solderprofile:



Tape & Reel (EIA-481-2-A)





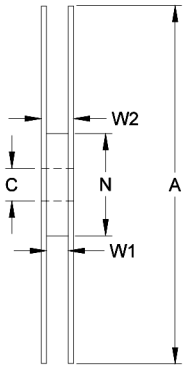


Table 7. Tape and Reel Information													
Tape Dimensions (mm)						**Reel Dimensions (mm)**							
Dimension	**W**	**F**	**Do**	**Po**	**P1**	**A**	**B**	**C**	**D**	**N**	**W1**	**W2**	**# Per Reel**
Tolerance	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Min**	**Typ**	**Min**	**Min**	**Typ**	**Max**	
VS-702	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

Table 8. Standard Output Frequencies (MHz)							
155M520000	156M250000	160M000000	162M000000	175M000000	187M500000	200M000000	212M500000
240M000000	245M760000	250M000000	260M000000	268M800000	300M000000	311M040000	312M500000
320M000000	324M000000	350M000000	375M000000	384M000000	389M600000	400M000000	480M000000
491M520000	500M000000	531M250000	532M000000	533M000000	537M600000	622M080000	625M000000
635M040000	637M500000	640M000000	644M531300	657M421900	666M514300	669M326600	672M162700
690M569200	693M483000	704M380600	707M352700	720M000000	742M434700	768M000000	796M875000
800M000000	901M120000	1000M00000					

Ordering Information

VS-702- E C E - K X A N - xxxMxxxxxx

Product Family
VS: VCSO

Package
702: 5 x 7.5 x 2.0 mm

Input
E: 3.3 Vdc ±10%

Output
C: LVPECL (45/55% Symmetry)
D: LVDS (45/55% Symmetry)

Operating Temperature
T: 0/70°C
E: -40/85°C

Frequency in MHz

Performance Options
N: Standard
A: Improved Phase Noise

Enable/Disable
A: Enable High
C: Enable Low

Stability
X: Standard
E: ±20ppm Temperature Stability

Absolute Pull Range
K: ±50ppm

**Note: not all combination of options are available.*
Other specifications may be available upon request.

Example: VS-702-ECE-KXAN-622M080000

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Revision History

Revision Date	Approved	Description
Feb 12, 2014	SD	Updated VI Asia address.
July 7, 2015	VN	Changed current specification in Table 1 to reflect 70mA typical and 90mA maximum.