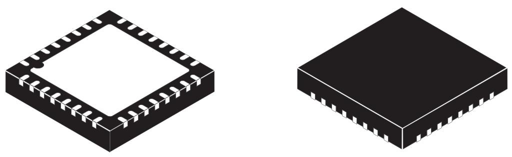
BlueNRG

Bluetooth® low energy wireless network processor

Datasheet - preliminary data



QFN32 (5 x 5 mm)

Features

- Bluetooth specification v4.0 compliant master and slave single-mode Bluetooth low energy network processor
- Embedded Bluetooth low energy protocol stack: GAP, GATT, SM, L2CAP, LL, RF-PHY
- Bluetooth low energy profiles provided separately
- Operating supply voltage: from 2.0 to 3.6 V
- 8.2 mA maximum TX current (@0 dBm, 3.0 V)
- Down to 1.7 µA current consumption with active BLE stack
- Integrated linear regulator and DC-DC step-down converter
- Up to +8 dBm available output power (at antenna connector)
- Excellent RF link budget (up to 96 dB)
- Accurate RSSI to allow power control
- Integrated general-purpose ADC
- Proprietary application controller interface (ACI), SPI based, allows interfacing with an external host application microcontroller
- Full link controller and host security
- High performance, ultra-low power Cortex-M0 32-bit based architecture core
- On-chip non-volatile Flash memory
- AES security co-processor
- Low power modes
- 16 or 32 MHz crystal oscillator
- 12 MHz ring oscillator
- 32 kHz crystal oscillator
- 32 kHz ring oscillator
- Battery voltage monitor and temperature sensor
- Compliant with the following radio frequency regulations: ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15, ARIB STD-T66
- Available in QFN32 (5 x 5 mm) package
- Operating temperature range: -40 °C to 85 °C

Applications

- Watches
- Fitness, wellness and sports
- Consumer medical
- Security/proximity
- Remote control
- Home and Industrial automation
- Assisted living
- Mobile phone peripherals
- PC peripherals

Table 1. Device summary

Order code	Package	Packing
BLUENRGQTR	QFN32	Tape and reel

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Contents

Description

The BlueNRG is a very low power Bluetooth low energy (BLE) single-mode network processor, compliant with Bluetooth specification v4.0. The BlueNRG can act as master or slave.The entire Bluetooth low energy stack runs on the embedded Cortex M0 core. The non-volatile Flash memory allows on-field stack upgrading. The BlueNRG allows applications to meet of the tight advisable peak current requirements imposed with the use of standard coin cell batteries. The maximum peak current is only 10 mA at 1 dBm of output power. Ultra low-power sleep modes and very short transition times between operating modes allow very low average current consumption, resulting in longer battery life. The BlueNRG offers the option of interfacing with external microcontrollers using SPI transport layer.

The BlueNRG integrates a general-purpose low-power ADC.

1 General description

The BlueNRG is a single-mode Bluetooth low energy master/slave network processor, compliant with the Bluetooth specification v4.0.

It integrates a 2.4 GHz RF transceiver and a powerful Cortex-M0 microcontroller, on which a complete power-optimized stack for Bluetooth single mode protocol runs, providing:

- full master and slave role support
- GAP: central, peripheral, observer or broadcaster roles
- ATT/GATT: client and server
- SM: privacy, authentication and authorization
- L2CAP
- Link Layer: AES-128 encryption and decryption

An on-chip non-volatile Flash memory allows on-field Bluetooth low energy stack upgrade.

The BlueNRG is equipped with Bluetooth low energy profiles in C source code.

The device allows applications to meet of the tight advisable peak current requirements imposed with the use of standard coin cell batteries. If the high efficiency embedded DC-DC step-down converter is used, the maximum input current is only 15 mA at the highest output power (+8 dBm). Even if the DC-DC converter is not used, the maximum input current is only 29 mA at the highest output power, still preserving battery life.

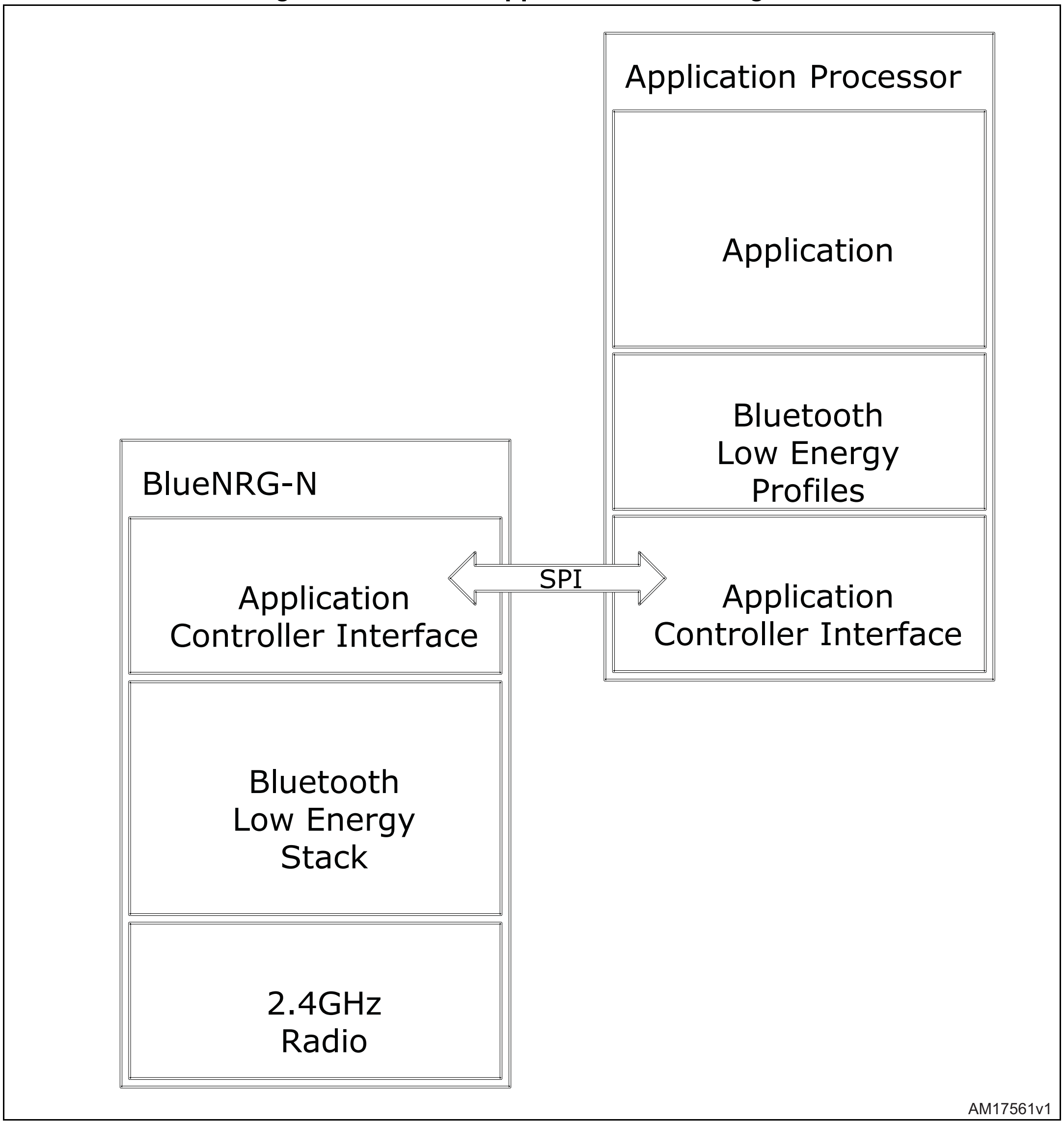
Ultra low-power sleep modes and very short transition time between operating modes result in very low average current consumption during real operating conditions, providing very long battery life.

Two different external matching networks are suggested: standard mode (TX output power up to +5 dBm) and high power mode (TX output power up to +8 dBm).

The external host application processor, where the application resides, is interfaced with the BlueNRG through an application controller interface protocol which is based on a standard SPI interface.

the BlueNRG integrates a low-power ADC. The input can be selected as single-ended or differential. It can also be used in conjunction with both a battery voltage level monitor and a temperature sensor. Either the battery voltage level or the temperature measurement may be made available to an external application controller through the application controller interface.

Figure 1. BlueNRG application block diagram



2 Pin description

The BlueNRG pinout is shown in *Figure 2*. In *Table 2* a short description of the pins is provided.

Figure 2. BlueNRG pinout top view (preliminary)

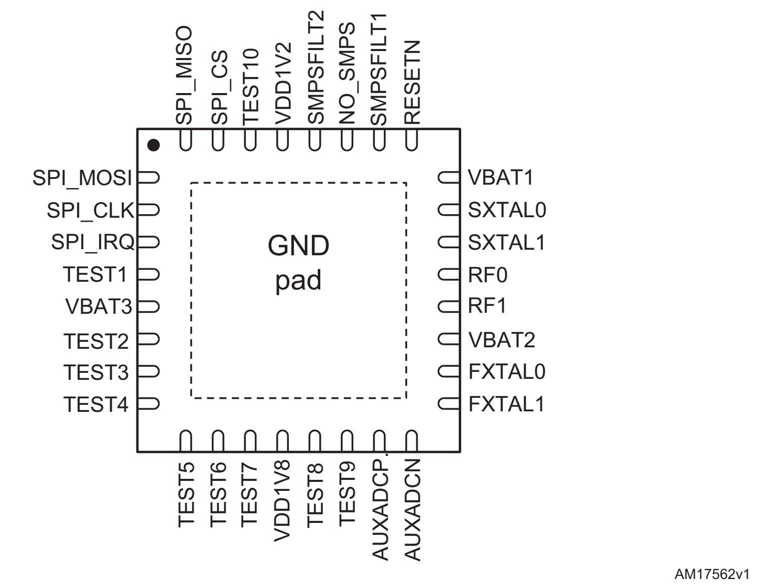


Table 2. Pinout description

Pin	Name	I/O	Description
1	SPI_MOSI	I/O	SPI_MOSI
2	SPI_CLK	I/O	SPI_CLK
3	SPI_IRQ	I/O	SPI_IRQ
4	TEST1	I/O	Test pin connected to GND
5	VBAT3	VDD	2.0-3.6 battery voltage input
6	TEST2	I/O	Test pin connected to GND
7	TEST3	I/O	Test pin connected to GND
8	TEST4	I/O	Test pin connected to GND
9	TEST5	I/O	Test pin connected to GND
10	TEST6	I/O	Test pin connected to GND
11	TEST7	I/O	Test pin connected to GND
12	VDD1V8	O	1.8 V Digital core
13	TEST8	O	Test pin not connected
14	TEST9		Test pin not connected
15	AUXADCP	I	Auxiliary ADC positive input

Table 2. Pinout description (continued)

Pin	Name	I/O	Description
16	AUXADCN	I	Auxiliary ADC negative input
17	FXTAL1	I	16/32 MHz crystal
18	FXTAL0	I	16/32 MHz crystal
19	VBAT2	VDD	2.0-3.6 battery voltage input
20	RF1	I/O	Antenna + matching circuit
21	RF0	I/O	Antenna + matching circuit
22	SXTAL1	I	32 kHz Crystal
23	SXTAL0	I	32 kHz Crystal
24	VBAT1	VDD	2.0-3.6 battery voltage input
25	RESETN	I	Reset and deep sleep control
26	SMPSFILT1	I/O	SMPS input
27	NO_SMPS	I	Power management strategy selection
28	SMPSFILT2	I/O	SMPS output
29	VDD1V2	O	1.2 V digital core
30	TEST10	I/O	TEST pin connected to GND
31	SPI_CS	I/O	SPI_CS
32	SPI_MISO	I/O	SPI_MISO

3 Application circuits

Figure 3. BlueNRG application circuit: active DC-DC converter

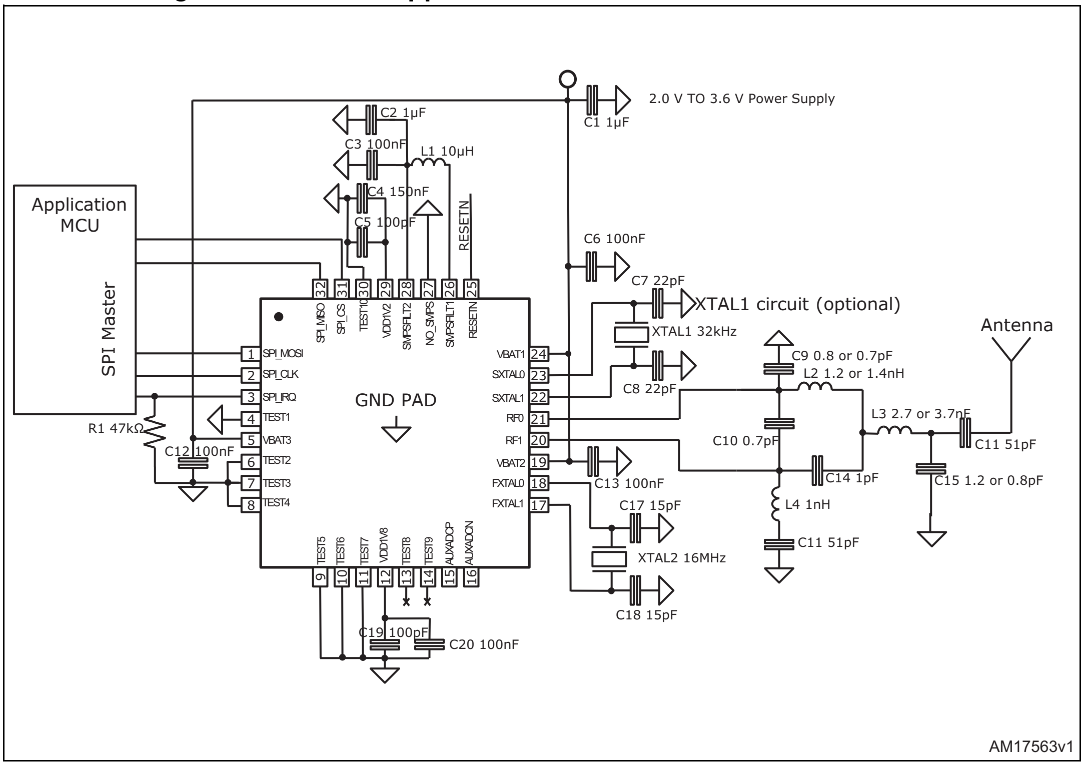


Figure 4. BlueNRG application circuit: non active DC-DC converter

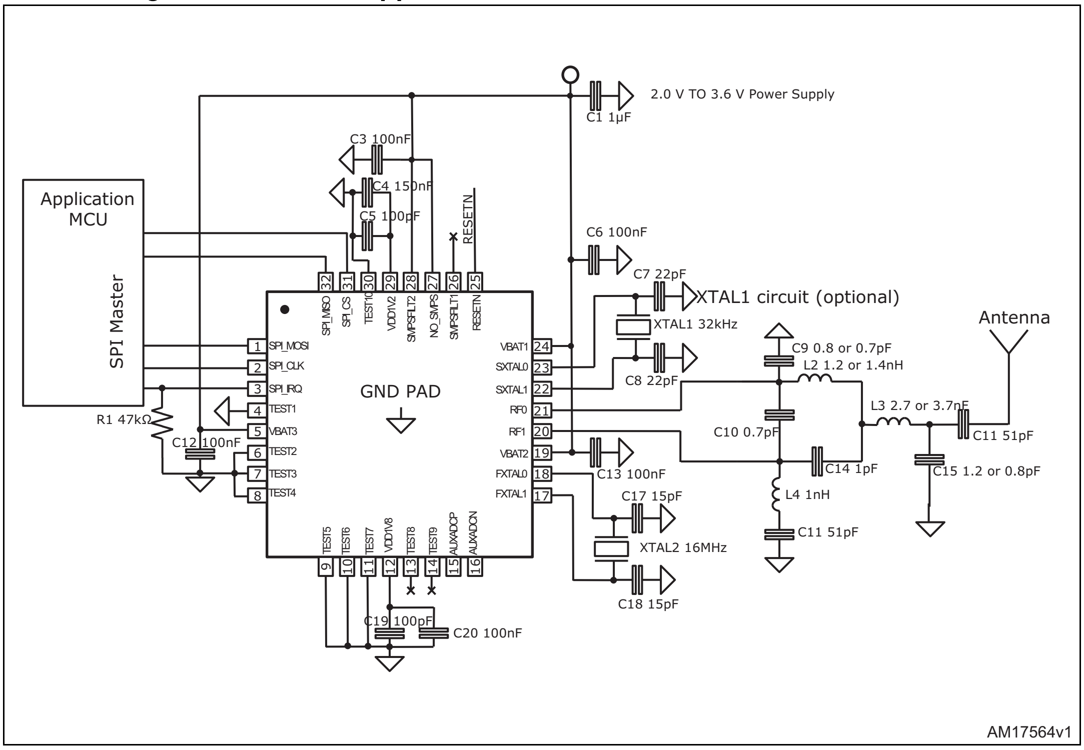


Table 3. External component list

Component	Description	Value
C1	Decoupling capacitor	1 µF
C2	DC-DC converter output capacitor	1 µF
C3	DC-DC converter output capacitor	100 nF
C4	Decoupling capacitor for 1.2 V digital regulator	150 nF
C5	Decoupling capacitor for 1.2 V digital regulator	100 pF
C6	Decoupling capacitor	100 nF
C7	32 kHz crystal loading capacitor	22 pF
C8	32 kHz crystal loading capacitor	22 pF
C9	RF balun/matching network capacitor High Performance RF balun/matching network capacitor Standard mode	0.8 pF 0.7 pF
C10	RF balun/matching network capacitor High Performance RF balun/matching network capacitor Standard mode	0.7 pF 0.7 pF
C11	RF balun/matching network capacitor High Performance RF balun/matching network capacitor Standard mode	51 pF 51 pF
C12	Decoupling capacitor	100 pF
C13	Decoupling capacitor	100 pF
C14	RF balun/matching network capacitor High Performance RF balun/matching network capacitor Standard mode	1p F 1p F
C15	RF balun/matching network capacitor High Performance RF balun/matching network capacitor Standard mode	1.2 pF 0.8 pF
C16	RF balun/matching network capacitor High Performance RF balun/matching network capacitor Standard mode	51 pF 51 pF
C17	16/32 MHz crystal loading capacitor	15 pF
C18	16/32 MHz crystal loading capacitor	15 pF
C19	Decoupling capacitor for 1.8 V digital regulator	100 pF
C20	Decoupling capacitor for 1.8 V digital regulator	100 nF
L1	DC-DC converter input inductor	10 µH
L2	RF balun/matching network inductor High Performance RF balun/matching network inductor Standard mode	1.2 nH 1.4 nH
L3	RF balun/matching network inductor High Performance RF balun/matching network inductor Standard mode	2.7 nH 3.7 nH
L4	RF balun/matching network inductor High Performance RF balun/matching network inductor Standard mode	1 nH 1 nH
R1	Pull-down resistor on the SPI_IRQ line (can be replaced by the internal pull-down of the Application MCU)	47 kΩ
XTAL1	32 kHz crystal (optional)	
XTAL2	16/32 MHz crystal	

4 Absolute maximum ratings and thermal data

Table 4. Absolute maximum ratings

Pin	Parameter	Value	Unit
5, 19, 24, 26, 28	DC-DC converter supply voltage input and output	-0.3 to +3.9	V
12, 29	DC voltage on linear voltage regulator	-0.3 to +3.9	V
1, 2, 3, 4, 6, 7, 8, 9, 10, 11, 25, 27, 30, 31, 32	DC voltage on digital input/output pins	-0.3 to +3.9	V
13, 14, 15,16	DC voltage on analog pins	-0.3 to +3.9	V
17, 18, 22, 23	DC voltage on XTAL pins	-0.3 to +1.4	V
20, 21 (1)	DC voltage on RF pins	-0.3 to +1.4	V
T_{STG}	Storage temperature range	-40 to +125	°C
$V_{ESD-HBM}$	Electrostatic discharge voltage	±2.0	KV

1. +8 dBm input power at antenna connector in Standard mode, +11 dBm in High Power mode, with given reference design.

Note: Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referred to GND.

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal resistance junction-ambient	TBD	°C/W
R_{thj-c}	Thermal resistance junction-case	TBD	°C/W

5 General characteristics

Table 6. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{BAT}	Operating Battery supply voltage	2.0		3.6	V
T_A	Operating Ambient temperature range	-40		+85	°C

6 Electrical specification

6.1 Electrical characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to T_A = 25 °C, V_{BAT} = 3.0 V. All performance data are referred to a 50 W antenna connector, via reference design.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Power consumption when DC-DC converter active						
I_{BAT}	Supply current	Reset		5		nA
		Standby (Slave) Standby (Master)		1.3 2		µA
		Sleep 32kHz XO ON (Slave) 32kHz XO ON (Master) 32kHZ RO ON (Slave) 32kHZ RO ON (Master)		 1.7 2.4 2.8 3.5		µA
		Active CPU, flash and RAM off CPU, flash and RAM on		 2 3.3		mA
		RX High Power mode RX Standard mode		7.7 7.3		mA
		TX Standard mode +5dBm 0dBm -2dBm -6dBm -9dBm -12dBm -15dBm -18dBm TX High Power mode +8dBm +4dBm +2dBm -2dBm -5dBm -8dBm -11dBm -14dBm		 11 8.2 7.2 6.7 6.3 6.1 5.9 5.8 15.1 10.9 9 8.3 7.7 7.1 6.8 6.6		mA

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Power consumption when DC-DC converter not active						
I_{BAT}	Supply current	Reset		5		nA
		Standby (Slave) Standby (Master)		1.4 2		µA
		Sleep 32kHz XO ON (Slave) 32kHz XO ON (Master) 32kHZ RO ON (Slave) 32kHZ RO ON (Master)		 1.7 2.4 2.8 3.5		µA
		Active CPU, flash and RAM off		 2.3		mA
		RX High Power mode RX Standard mode		14.5 14.3		mA
		TX Standard mode +5dBm 0dBm -2dBm -6dBm -9dBm -12dBm -15dBm -18dBm TX High Power mode +8dBm +4dBm +2dBm -2dBm -5dBm -8dBm -11dBm -14dBm		 21 15.4 13.3 12.2 11.5 11 10.6 10.4 28.8 20.5 17.2 15.3 14 13 12.3 12		mA
Digital SPI input and output (SPI_MISO, SPI_MOSI, SPI_CLK, SPI_IRQ and RESET)						
C_{IN}	Port I/O capacitance		1.29	1.38	1.67	pF
T_{RISE}	Rise time	0.1*VDD to 0.9*VDD, CL=50pF	5		19	ns
T_{FALL}	Fall time	0.9*VDD to 0.1*VDD, CL=50pF	6		22	ns
V_{IH}	Logic high level input voltage		0.65 VDD			
V_{IL}	Logic low level input voltage				0.35 VDD	
V_{OH}	High level output voltage (ULPI port)	VDD = 3.3 V	2.4			V
V_{OL}	Low level output voltage (ULPI port)	VDD = 3.3 V			0.4	V

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Digital SPI input SPI_CS						
C_{IN}	Port I/O capacitance		1.29	1.38	1.67	pF
C_{IN}	Port I/O capacitance		1.29	1.38	1.67	pF
T_{RISE}	Rise time	0.1*VDD to 0.9*VDD, CL=50pF	5.05		18.5	ns
T_{FALL}	Fall time	0.9*VDD to 0.1*VDD, CL=50pF	5.647		21.93	ns
V_{IH}	Logic high level input voltage		0.65 VDD			
V_{IL}	Logic low level input voltage				0.35 VDD	

6.2 RF general characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to T_A = 25 °C, V_{BAT} =3.0 V. All performance data are referred to a 50 Ω antenna connector, via reference design.

Table 8. RF general characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
FREQ	Frequency range		2400		2483.5	MHz
F_{CH}	Channel spacing			2		MHz
RF_{ch}	RF channel center frequency		2402		2480	MHz

6.3 RF transmitter characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to T_A = 25 °C, V_{BAT} = 3.0 V. All performance data are referred to a 50 Ω antenna connector, via reference design.

Table 9. RF Transmitter characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
MOD	Modulation scheme		GFSK			
BT	Bandwidth-bit period product			0.5		
M_{index}	Modulation index		0.45	0.5	0.55	
DR	Air data rate			1		Mbps
ST_{acc}	Symbol time accuracy				50	ppm
P_{MAX}	Maximum Output Power High Power Standard mode	At antenna connector		+8 +5	+10 +7	dBm
P_{RFC}	Minimum Output Power High Power Standard mode			-15 -18		dB
P_{RFC}	RF power accuracy				±2	dB
P_{BW1M}	6 dB Bandwidth for modulated carrier (1 Mbps)	Using resolution bandwidth of 100kHz	500			kHz
P_{RF1}	1st Adjacent channel transmit power 2 MHz	Using resolution bandwidth of 100 kHz and average detector			-20	dBm
P_{RF2}	2nd Adjacent channel transmit Power >3MHz	Using resolution bandwidth of 100 kHz and average detector			-30	dBm
P_{SPUR}	Spurious emission	Harmonics included. Using resolution bandwidth of 1 MHz and average detector			-41	dBm
CF_{dev}	Center frequency deviation	During the packet and including both initial frequency offset and drift			±150	kHz
$Freq_{drift}$	Frequency drift	During the packet			±50	kHz
$IFreq_{drift}$	Initial carrier frequency drift				±20	kHz
$DriftRate_{max}$	Maximum drift rate				400	Hz/µs
Z_{LOAD}	Optimum differential load	Standard mode @ 2440 MHz High Power mode @ 2440 MHz		25.9 + j44.4 25.4 + j20.8		Ω

6.4 RF receiver characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to T_A = 25 °C, V_{BAT} =3.0 V. All performance data are referred to a 50 Ω antenna connector, via reference design.

Table 10. RF receiver characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RX_{SENS}	Sensitivity	BER <0.1%	-	-88		dBm
P_{SAT}	Saturation Standard mode High power mode	BER <0.1%	-	8 11		dBm
z_{IN}	Input differential impedance	Standard mode @ 2440 MHz High power mode @ 2440 MHz	-	31.4 - j26.6 28.8 - j18.5		Ω
RF selectivity with BLE equal modulation on interfering signal						
$C/I_{CO\text{-}channel}$	Co-channel interference	Wanted signal=-67dBm, BER≤0.1%	-	9		dBc
$C/I_{1\ MHz}$	Adjacent (+1 MHz) Interference	Wanted signal=-67dBm, BER≤0.1%	-	2		dBc
$C/I_{2\ MHz}$	Adjacent (+2 MHz) Interference	Wanted signal=-67dBm, BER≤0.1%	-	-34		dBc
$C/I_{3\ MHz}$	Adjacent (+3 MHz) Interference	Wanted signal=-67dBm, BER≤0.1%	-	-40		dBc
$C/I_{\geq 4\ MHz}$	Adjacent (≥±4 MHz) Interference	Wanted signal=-67dBm, BER≤0.1%	-	-34		dBc
$C/I_{\geq 6\ MHz}$	Adjacent (≥±6 MHz Interference	Wanted signal=-67dBm BER≤0.1%	-	-45		dBc
$C/I_{\geq 25\ MHz}$	Adjacent (≥±25 MHz) Interference	Wanted signal=-67dBm, BER≤0.1%	-	-64		dBc
C/I_{Image}	Image frequency Interference -2MHz	Wanted signal=-67dBm, BER≤0.1%	-	-20		dBc
$C/I_{Image\pm 1\ MHz}$	Adjacent (±1 MHz) Interference to in-band image frequency -1MHz -3MHz	Wanted signal=-67dBm, BER≤0.1%	-	5 -25		dBc
Out of Band Blocking (Interfering signal CW)						
C/I_{Block}	Interfering signal frequency 30 MHz – 2000 MHz	Wanted signal=-67dBm, BER≤0.1%, Measurement resolution 10 MHz	-		-30	dBm
C/I_{Block}	Interfering signal frequency 2003 MHz – 2399 MHz	Wanted signal=-67dBm, BER≤0.1%, Measurement resolution 3 MHz	-		-35	dBm

Table 10. RF receiver characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C/I_{Block}	Interfering signal frequency 2484 MHz – 2997 MHz	Wanted signal=-67 dBm, BER≤0.1%, measurement resolution 3 MHz	-		-35	dBm
C/I_{Block}	Interfering signal frequency 3000 MHz – 12.75 GHz	Wanted signal=-67dBm, BER≤0.1%, measurement resolution 25 MHz			-30	dBm
Intermodulation characteristics (CW signal at f_1, BLE interfering signal at f_2)						
P_IM(3)	Input power of IM interferes at 3 and 6 MHz distance from wanted signal	Wanted signal=-64dBm, BER≤0.1%	-	-33		dBm
P_IM(-3)	Input power of IM interferes at -3 and -6 MHz distance from wanted signal	Wanted signal=-64dBm, BER≤0.1%		-43		dBm
P_IM(4)	Input power of IM interferes at ±4 and ±8 MHz distance from wanted signal	Wanted signal=-64dBm, BER≤0.1%		-33		dBm
P_IM(5)	Input power of IM interferes at ±5 and ±10 MHz distance from wanted signal	Wanted signal=-64dBm, BER≤0.1%		-33		dBm

6.5 High speed crystal oscillator (HSXOSC) characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to T_A = 25 °C, V_{BAT} = 3.0 V.

Table 11. High speed crystal oscillator characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal frequency			16/32		MHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance.			±50	ppm
C_L	Load capacitance			15/TBD		pF
ESR	Equivalent series resistance				100	Ω
P_D	Drive level				100	µW

6.6 Low speed crystal oscillator (LSXOSC) characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to T_A = 25 °C, V_{BAT} =3.0 V.

Table 12. Low speed crystal oscillator characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal frequency			32.768		kHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance.			±50	ppm
C_L	Load capacitance			22		pF
ESR	Equivalent series resistance				90	kΩ
P_D	Drive level				0.1	µW

6.7 High speed ring oscillator (LSROSC) characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to T_A = 25 °C, V_{BAT} =3.0 V.

Table 13. High speed ring oscillator characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal Frequency			12	16	MHz

6.8 Low speed ring oscillator (LSROSC) characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to T_A = 25 °C, V_{BAT} =3.0 V.

Table 14. Low speed ring oscillator characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
32 kHz ring oscillator (LSROSC)						
f_{NOM}	Nominal frequency			37.4		kHz
f_{TOL}	Frequency tolerance				±500	ppm

6.9 N-fractional frequency synthesizer characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to T_A = 25 °C, V_{BAT} =3.0 V, f_c = 2440 MHz.

Table 15. Low speed ring oscillator characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PN_{SYNTH}	RF carrier phase noise	At ±1MHz offset from carrier		-113		dBc/Hz
		At ±3MHz offset from carrier		-119		dBc/Hz
		At ±6MHz offset from carrier		TBD		dBc/Hz
		At ±25MHz offset from carrier		TBD		dBc/Hz
$LOCK_{TIME}$	PLL lock time				40	µs
TO_{TIME}	PLL turn on / hop time	Including calibration			150	µs
PN_{SYNTH}	RF carrier phase noise	At ±1MHz offset from carrier		-113		dBc/Hz

6.10 Auxiliary blocks characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to T_A = 25 °C, V_{BAT} =3.0 V, f_c = 2440 MHz.

Table 16. Low speed ring oscillator characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Analog Temperature Sensor						
T_{rERR}	Error in temperature	(after calibration)	-4	0	+4	^0C
T_{SLOPE}	Temperature coefficient			3.1		$mV/^0C$
T_{ICC}	Current consumption			10		µA
$T_{TS\text{-}OUT}$	Output voltage level			1		V
Battery indicator and brown-out Reset (BOR)						
V_{BLT1}	Battery level thresholds 1			2.7		V
V_{BLT2}	Battery level thresholds 2			2.5		V
V_{BLT3}	Battery level thresholds 3			2.3		V
V_{BLT4}	Battery level thresholds 4			2.1		V
A_{BLT}	Battery level thresholds accuracy				5	%
V_{ABOR}	Ascending brown-out threshold			1.79		V
V_{DBOR}	Descending brown-out threshold			1.73		V

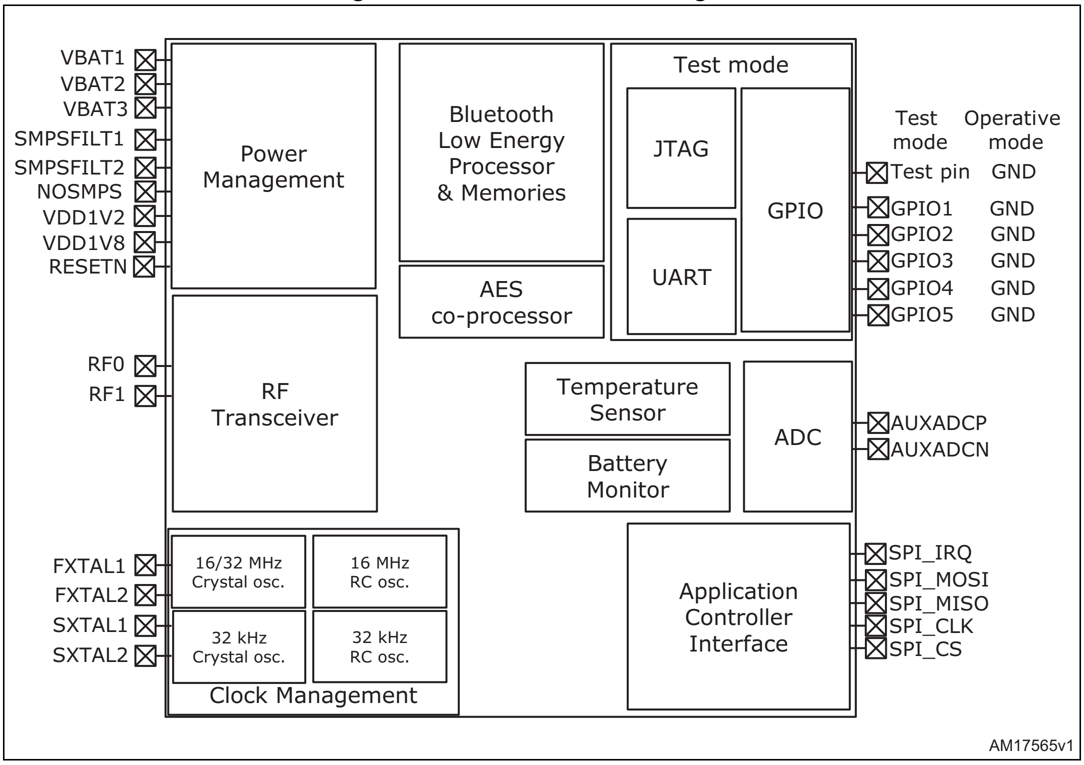
Table 16. Low speed ring oscillator characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Analog to digital converter (ADC)						
V_{DDA}	Analog supply voltage		2.0	3.0	3.6	V
$I_{DDA, AVG}$	Analog supply current	Average current during conversion			500	uA
$I_{DDA, OFF}$	Analog supply current	Block disabled		TBD		nA
$V_{INP, iNN}$	Input pin voltage		0.4		0.8	V
f_{CLK}	Clock frequency			1		MHz
T_{acq}	Acquisition time			1313		µs
N	Number of bits	Two's complement		TBD		bits

7 Block diagram and descriptions

A block diagram of the BlueNRG is shown in *Figure 5*. In the following subsections a short description of each module is given.

Figure 5. BlueNRG block diagram



7.1 Core, memory and peripherals

The BlueNRG contains an ARM Cortex-M0 microcontroller core that supports ultra-low leakage state retention mode and almost instantaneously returning to fully active mode on critical events.

The memory subsystem consists of 64 KB Flash, and 12 KB RAM. Flash is used for the M0 program. RAM is used for data.

In Test mode the IO controller handles the general-purpose I/O pins, which can be configured to be controlled by peripherals modules or by software. Each IO can be configured as an input or output and the different flavors of input and output. JTAG and UART are available only in Test mode.

The application controller interface (ACI) uses a standard SPI slave interface as transport layer, basing in five physical wires:

- 2 control wires (clock and slave select)
- 2 data wires with serial shift-out (MOSI and MISO) in full duplex
- 1 wire to indicate data availability from the slave

Table 17. SPI Interface

Name	Direction	Width	Description
SPI_CS	In	1	SPI slave select = SPI enable.
SPI_CLK	In	1	SPI clock (max 8 MHz).
SPI_MOSI	In	1	Master output, slave input.
SPI_MISO	Out	1	Master input, slave output.
SPI_IRQ	Out	1	Slave has data for master.

The BlueNRG integrates a temperature sensor to report the silicon temperature. The characteristics of the temperature sensor are defined in *Table 16*.

The device embeds a battery level detector to monitor the supply voltage. The characteristics of the battery level detector are defined in *Table 16*.

Dedicated ACI commands enable the integrated ADC to measure a voltage level at the AUXADCP and AUXADCN pins input. The ADC can also measure the temperature sensor output and the battery level. The characteristics of the auxiliary ADC are defined in *Table 16*.

7.2 Power management

The BlueNRG integrates both a low dropout voltage regulator (LDO) and a step-down DC-DC converter, and one of them can be used to power the internal BlueNRG circuitry. However even when the LDO is used, the stringent maximum current requirements, which are advisable when coin cell batteries are used, can be met and further improvements can be obtained with the DC-DC converter at the sole additional cost of an inductor and a capacitor.

The internal LDOs supplying both the 1.8 V digital blocks and 1.2 V digital blocks require decoupling capacitors for stable operation.

Figure 6 and *Figure 7*, show the simplified power management schemes using LDO and DC-DC converter.

Figure 6. Power management strategy using LDO

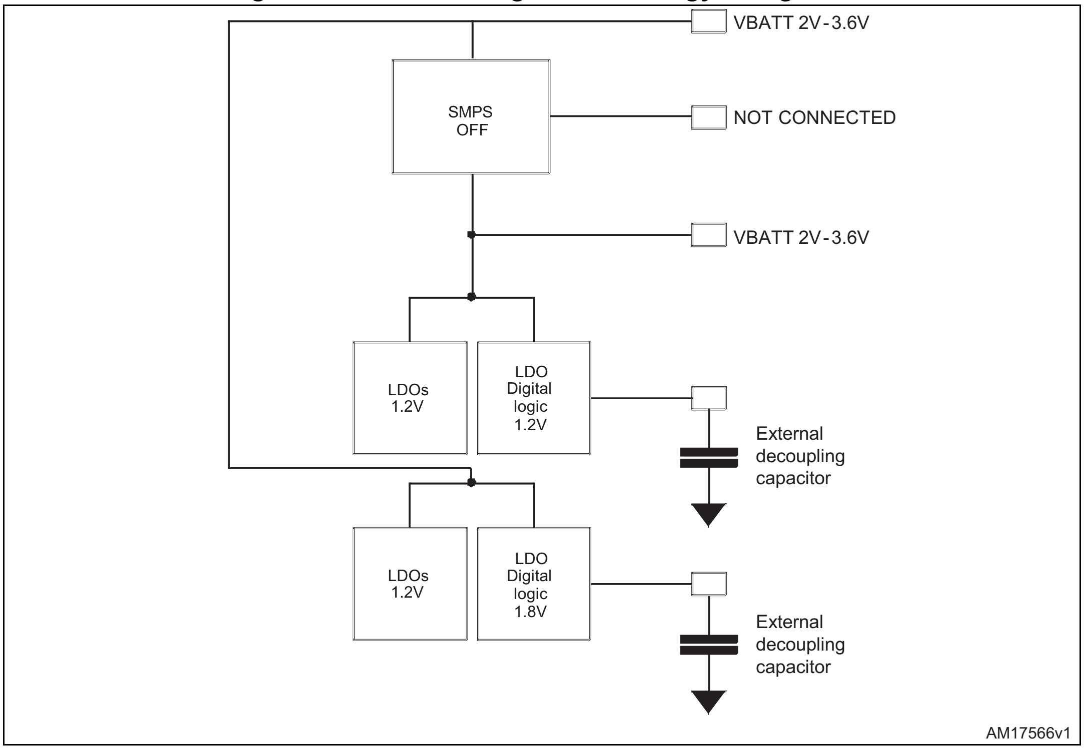
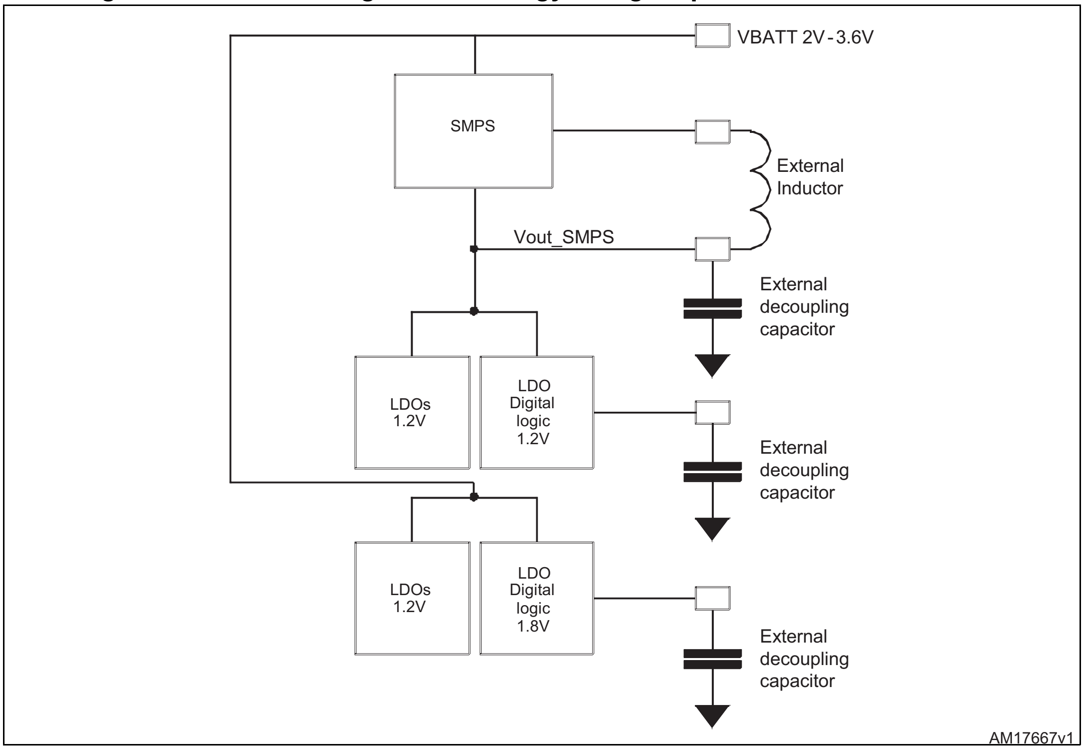


Figure 7. Power management strategy using step-down DC-DC converter



7.3 Clock management

The BlueNRG integrates two low-speed frequency oscillators (LSOSC) and two High speed (16 MHz or 32 MHz) frequency oscillators (HSOSC).

The low frequency clock is used in Low Power mode and can be supplied either by a 32.7 kHz oscillator that uses an external crystal and guarantee up to ±50 ppm frequency tolerance, or by a ring oscillator with maximum ±500 ppm frequency tolerance, which does not require any external components.

The primary high frequency clock is a 16 MHz or 32 MHz crystal oscillator. There is also a fast-starting 12 MHz ring oscillator that provides the clock while the crystal oscillator is starting up. Frequency tolerance of high speed crystal oscillator is ±50 ppm.

7.4 Bluetooth low energy radio

The BlueNRG integrates a RF transceiver compliant to the Bluetooth specification and to the standard national regulations in the unlicensed 2.4 GHz ISM band.

The RF transceiver requires very few external discrete components. It provides 96 dB link budgets with excellent link reliability, keeping the maximum peak current below 15 mA.

In Transmit mode, the power amplifier (PA) drives the signal generated by the frequency synthesizer out to the antenna terminal through a very simple external network. The power delivered as well as the harmonic content depends on the external impedance seen by the PA.

The output power is programmable from -18 dBm to +8 dBm, to allow a user-defined power control system and to guarantee optimum power consumption for each scenario.

8 Operating modes

Several operating modes are defined for the BlueNRG:

- Reset mode
- Sleep mode
- Standby mode
- Active mode
- Radio mode
  - Receive Radio mode
  - Transmit Radio mode

In Reset mode, the BlueNRG is in ultra-low power consumption: all voltage regulators, clocks and the RF interface are not powered. The BlueNRG enters Reset mode by asserting the external reset signal. As soon as it is de-asserted, the device follows the normal activation sequence to transit to Active mode.

In Sleep mode either the low speed crystal oscillator or the low speed ring oscillator are running, whereas the high speed oscillators are powered down as well as the RF interface. The state of the BlueNRG is retained and the content of the RAM is preserved.

While in Sleep mode, the BlueNRG waits until an internal timer expires and then it goes into Active mode. The transition from Sleep mode to Active mode can also be activated through the SPI interface.

Standby mode and Sleep mode are equivalent but the low speed frequency oscillators are powered down. In Standby mode the BlueNRG can be activated through the SPI interface.

In Active mode the BlueNRG is fully operational: all interfaces, including SPI and RF, are active as well as all internal power supplies together with the high speed frequency oscillator. The MCU core is also running.

Radio mode differs from Active mode as also the RF transceiver is active and it is capable of either transmitting or receiving.

Figure 8 reports the simplified state machine:

Figure 8. Simplified state machine

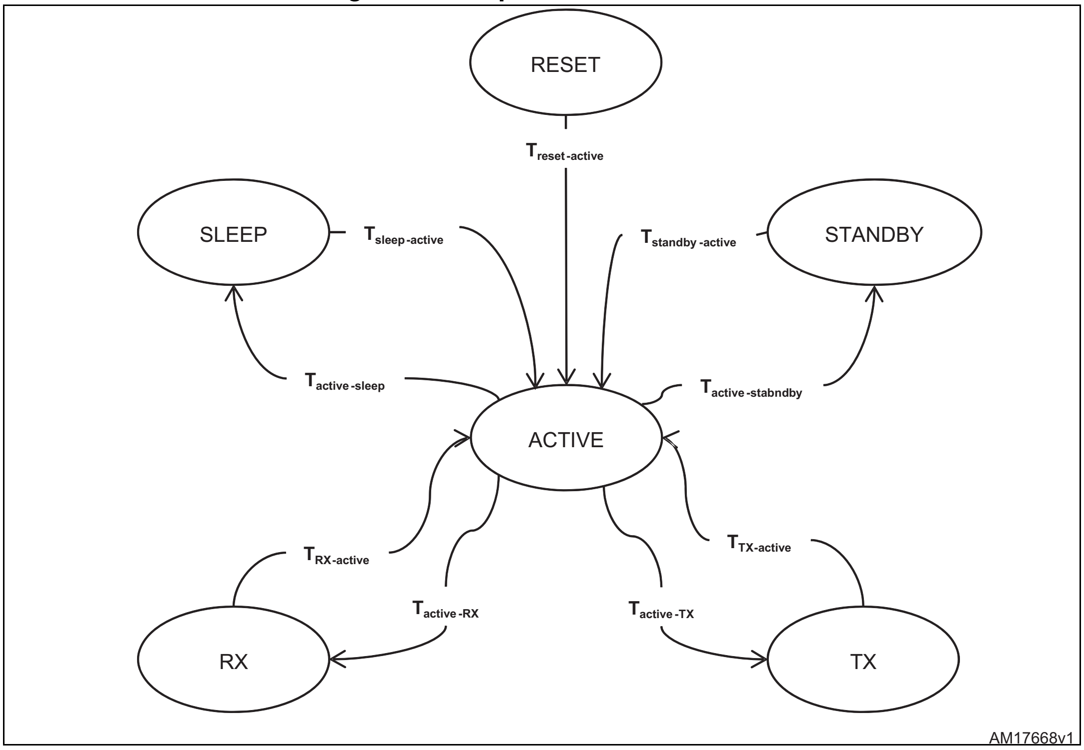


Table 18. BlueNRG operating modes

State	Digital LDO	SPI	LSOSC	HSOSC	Core	RF synt.	RX chain	TX chain
Reset	OFF Register contents lost	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Standby	ON Register contents retained	ON	OFF	OFF	OFF	OFF	OFF	OFF
Sleep	ON Register contents retained	ON	ON	OFF	OFF	OFF	OFF	OFF
Active	ON Register contents retained	ON	-	ON	ON	OFF	OFF	OFF
RX	ON Register contents retained	ON	-	ON	ON	ON	ON	OFF
TX	ON Register contents retained	ON	-	ON	ON	ON	OFF	ON

Table 19. BlueNRG transition times

Transition	Maximum time	Condition
Reset-active	1.5 ms	32 kHz not available
	7 ms	32 kHz RO
	94 ms	32 kHz XO
Standby-active	0.42 ms	32 kHz not available
	6.2 ms	32 kHz RO
	93 ms	32 kHz XO
Sleep-active	0.42 ms	
Active-RX	125 µs	Channel change
	61 µs	No channel change
Active-TX	131 µs	Channel change
	67 µs	No channel change
RX-TX or TX-RX	150 µs	

9 Application controller interface

The application controller Interface is based on a standard SPI module with speeds up to 8 MHz. The application controller Interface defines a software protocol providing functions to access all the services offered by the layers of the embedded Bluetooth stack. The ACI commands are described in the BlueNRG ACI command interface document.

10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 9. QFN32 (5 x 5 x 1 pitch 0.5 mm) drawing

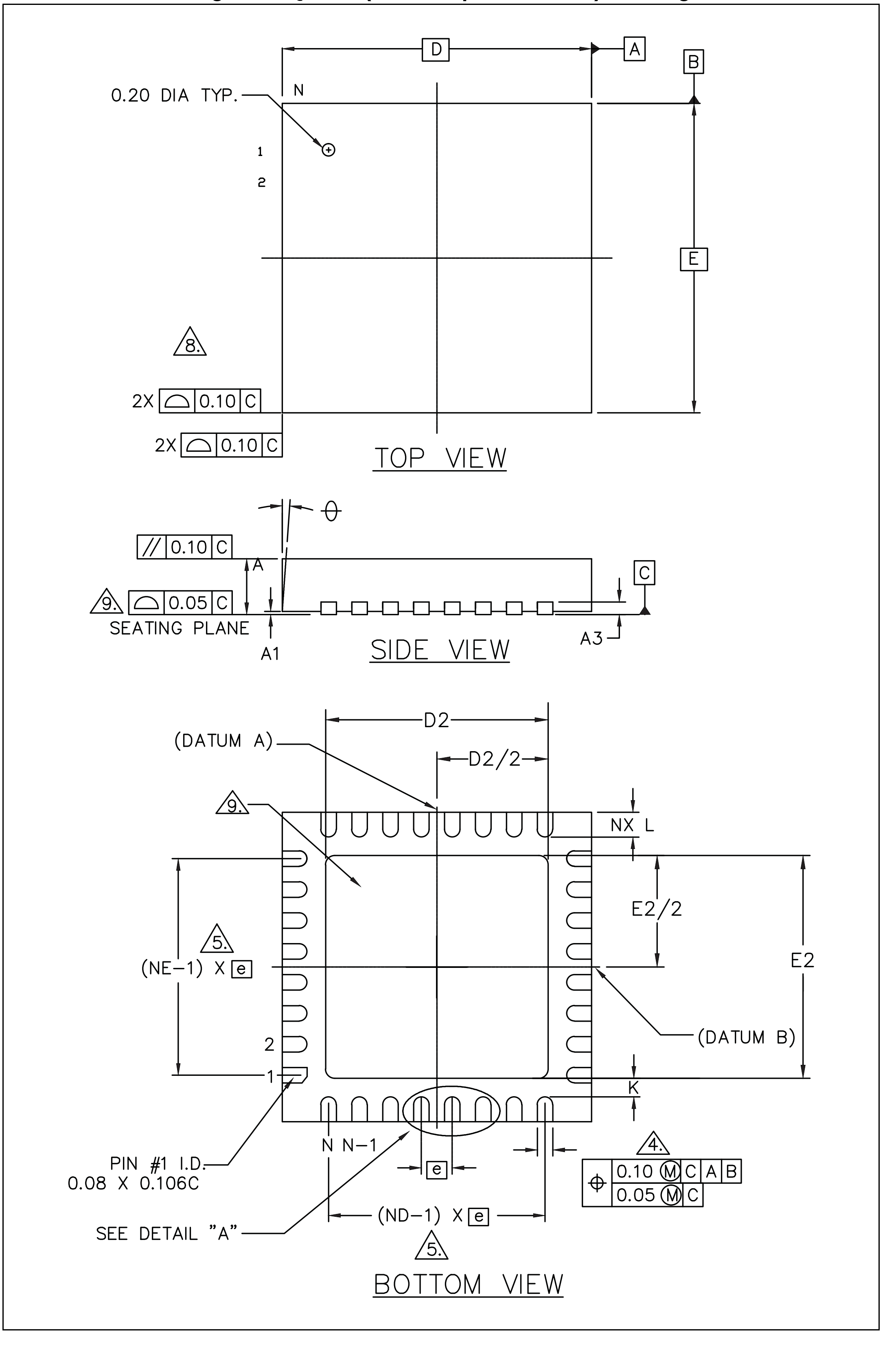


Table 20. QFN32 (5 x 5 x 1 pitch 0.5 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.85	1.00
A1	0	0.02	0.05
A3	0.20 REF		
b	0.25	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
D2	3.2		3.70
E2	3.2		3.70
e	5.00 BSC		
L	0.30	0.40	0.50
Φ	0°		14°
K	0.20		

11 Revision history

Table 21. Document revision history

Date	Revision	Changes
09-Aug-2013	1	Initial release.