Sampling Phase Detectors

Sampling Phase Detector Modules

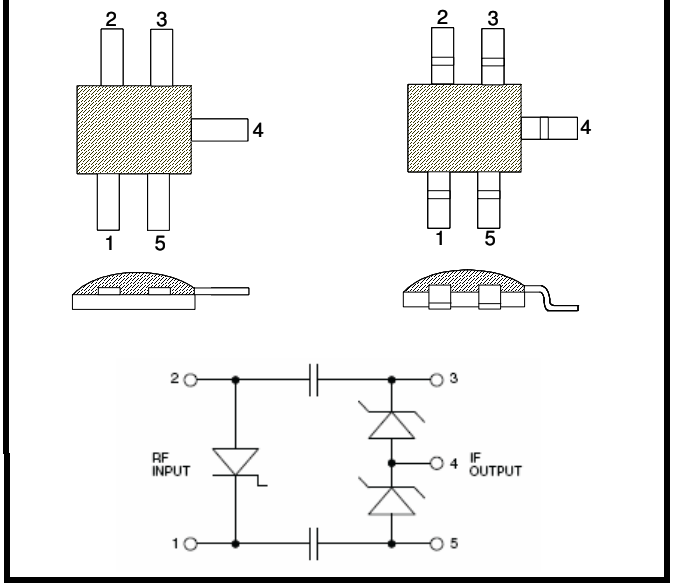
DESCRIPTION

The Sampling Phase Detector (SPD) module is a hybrid circuit providing a fast Step Recovery Diode, coupling capacitors and a low barrier Schottky pair. The Schottky pair is used as a sampling circuit turned on by the fast step from the Step Recovery Diode, or in the frequency domain, the Schottkys act as a mixer to mix the harmonic of the SRD step closest to the microwave frequency. The output is a beat frequency (the difference between the harmonic of the reference and the microwave frequency) and is just a DC voltage at the lock point. It is used to phase lock DRO's and VCO's from 10 to 1000 MHz (TYP) reference frequencies.

LEAD FREE RoHS COMPLIANT

PACKAGE STYLE & SCHEMATIC

E50 & E50SM



FEATURES

- Phase Locking to 22 GHz
- Broadband Capability
- Fully Integrated Module
- Phase Locks DRO's and VCO's

MAXIMUM RATINGS

Storage Temperature . . . . . -65 to +150 °C
Operating Temperature . . . . . -65 to +150 °C
Soldering Temperature . . . . . 230 °C for 5 sec
ESD Rating . . . . . HBM, Class 0

ELECTRICAL CHARACTERISTICS T_C = +25°C

Part Number	Microwave Freq		Cap	Step Recovery Diode					Schottky Sampling Diodes		
	Power Drive Max dBm	Range Max GHz	pF	F_{REF} Min MHz	P_{REF} Range dBm	C_{T-6} TYP pF	T_L TYP nS	T_T TYP pS	C_{T0} TYP pF	$V_{F\ 1\ mA}$ TYP mV	R_{DS} TYP Ohms
MSPD-1000-E50(1)	+7	0.5	18 - 22	10	17 to 27	1.10	35	65	.40	250	7
MSPD-1002-E50(1)	+7	2.5	3 - 4.1	25	17 to 27	0.76	20	50	.36	250	8
MSPD-1012-E50(1)	+6	12.5	2 - 3.1	50	17 to 27	0.85	10	35	.32	250	9
MSPD-2018-E50(1)	+4	22	.45 - 0.7	100	17 to 23	0.50	6	45	.23	425	16

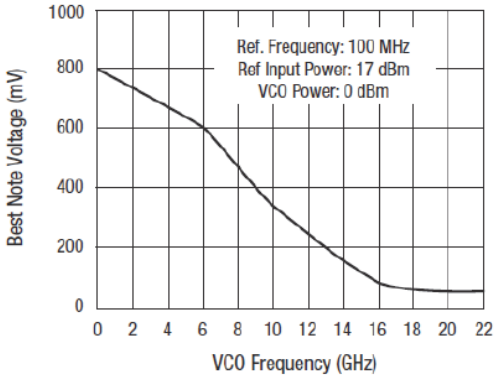
Notes:
1. Surface mount package E50SM is also available.

975 Stewart Drive, Sunnyvale, CA 94085 PH 408.737.8181 FAX: 408.733.7645

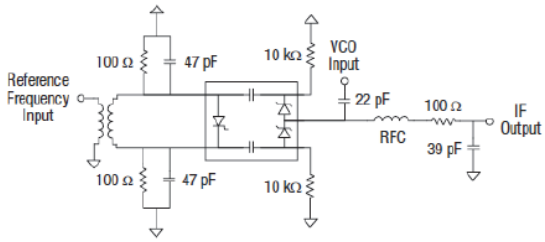
Rev. 03/12/2012

MSPD1012-E50

Typical Performance

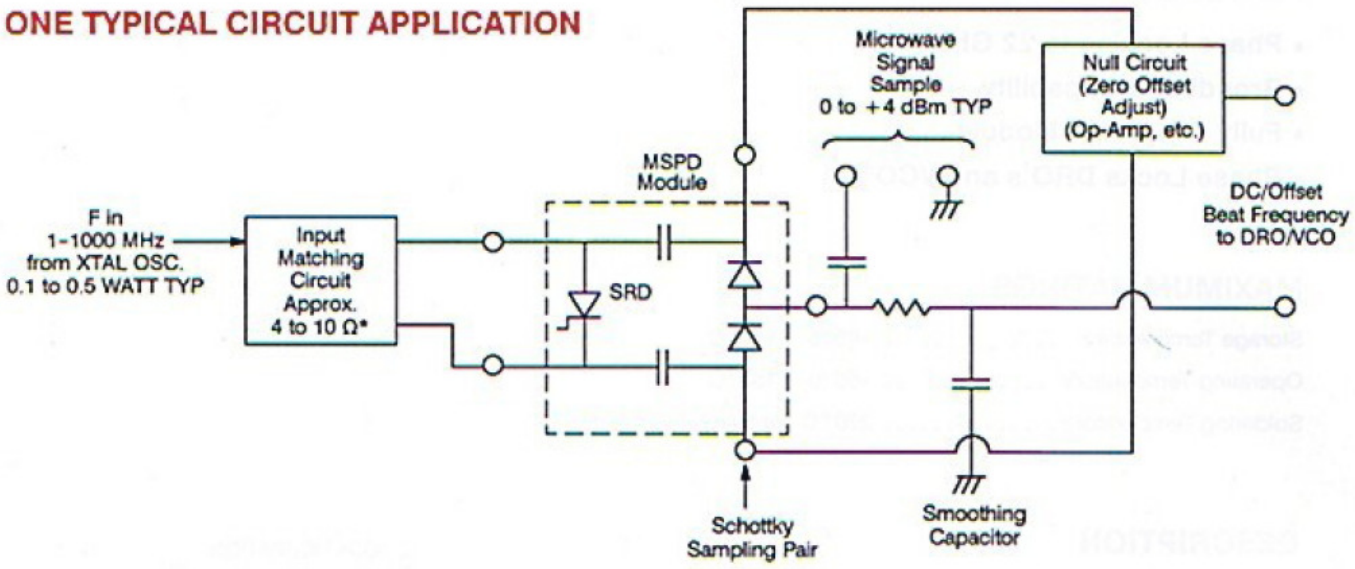


Recommended Circuit



Input transformer: 10:1 step down impedance ratio.

ONE TYPICAL CIRCUIT APPLICATION



Note: All circuits have broadband capability and are not limited to the frequencies stated.

Sampling Phase Detectors

The Sampling Phase Detector (SPD) is composed of a comb generator, a coupling network and a single balanced mixer. It is designed to be used in phase locking circuits for microwave oscillators.

The following description of the operation of the SPD refers to Figure 1. The step recovery diode (SRD) D1 charges during the forward bias part of the AC cycle. The charge is withdrawn during the reverse bias part of the AC cycle, and D1 transitions, producing an edge. The capacitors C1 and C2 differentiate the edge into an impulse and apply this impulse to the schottky diodes D2 and D3, which are turned on briefly and apply a sample of the microwave signal to the IF filter. When the reference signal and the microwave signal are harmonically related, the same voltage point on the microwave signal is applied to the IF filter, producing a steady DC output or offset voltage. When the two signals are not exactly related, a different point on the microwave signal is applied to the IF filter each cycle, producing a sine wave with a frequency that is equal to the difference between the microwave signal's frequency and the frequency of the closest harmonic of the reference signal. This frequency is also defined as the difference frequency.

The design criteria for the circuit, shown in Figure 2, is described below. Transformer T1 matches the reference oscillator to the SRD and converts the oscillator's signal from single ended to balanced. The SPD requires +17 dBm to + 27 dBm from the reference oscillator to work properly. The SRD impedance, which is about 50 ohms at +17 dBm, decreases as the drive level is increased. R1 and R2, each of which should be about 50 ohms, provide a termination for the microwave signal and dampen reflections in the SPD caused by mismatches. C1 isolates the IF signal from the microwave source. Its value should be chosen so it has a high impedance (at least 150 ohms) at the IF frequency and a low impedance (less then 10 ohms) at the microwave frequency. C1 can be replaced by a high pass or bandpass filter network. The circuit's performance can be improved by matching the microwave source to the Schottky diodes. Also use microwave layout rules for the physical layout of the interface circuit between the microwave source and the Schottkys. R3 and C2 create a low pass filter which separates out the IF signal. The cut off frequency of this filter should be selected to block the next higher harmonic of the reference oscillator. For example, the harmonics of a 100 MHz reference occur every 100 MHz, the cut off frequency must be less then 100 MHz. R3 may be replaced by an inductor of an appropriate value. Care must be taken not to shunt the microwave signal away from the Schottkys with a low quality inductor. R4, R5 and R6 provide the return path for the IF signal. R4 provides a DC offset adjustment. R5 and R6 should have a value of at least 100 ohms and be placed as close to the SPD as possible. R5 and R6 keep the impulse and microwave signal inside the SPD. Figure 3 shows an alternative IF return network with R4 removed. The resistors R5 and R6 can be replaced with low pass filters. The low pass filters need to present a high impedance (Z>200 ohms) to the SPD to keep from loading down the impulse and microwave signal.

There are four models of the SPD shown in the Metelics catalog. Each one is designed to work at a particular microwave frequency. This maximum frequency is not a cut off frequency; but, it is a suggested upper limit based on the Schottky's junction capacitance. For the MSPD-1002 and MSPD-1000, the transition time of the SRD will limit the upper frequency to 4 GHz.

The circuit in Figure 2 is designed to work with a sine wave driving the SRD. The SRD can be driven with a square wave or a pulse. For low frequency (<20 MHz) references, a pulse drive will work better then sine wave drive. The minimum requirements is a forward bias cycle of at least 10 nS and a reverse bias cycle long enough to remove all the stored charge and allow the SRD to transition. The reverse bias cycle should have a fall time less then 0.8 nS. The maximum current in either direction should be 10 mA and the maximum reverse voltage should be 13 V. The greater the reverse voltage, the greater the impulse generated. One way to achieve pulse drive is shown in Figure 4. The circuit uses a constant current source to supply the forward bias. Then a pulse is superimposed to reverse bias the SRD. R is a minimum of 1000 ohms and C is 0.02 uF. The forward voltage drop of the SRD is about 1 V and varies about -2 mV/°C.

One property of the SPD is that the conversion efficiency varies approximately as $\sin(n\pi x) / (n\pi x)$. This is due to the impulse driving the Schottkys. Minimum conversion efficiency occurs when $(n\pi x) = N$ where n and N are integers. The value of X is controlled by the reference frequency and the value of the coupling capacitors. When testing a new design, adjusting the microwave frequency is recommended to insure the circuit is not at a minimum. If the circuit is at a minimum and the reference frequency cannot be changed, the coupling capacitance can be raised by adding external capacitors.

There are several ways to connect a single balanced mixer. The circuit in Figure 2 is based on the circuit shown in Figure 6. Figure 7 shows another possibility. When used as a sampling mixer, the SPD has a high

conversion loss (example: Fref = 100 MHz, Fmicrowave = 1 GHz and F_{IF} = 1 KHz, Conversion Loss = 25 dB).

Figure 8 shows how IF output varies with microwave power at various reference drive levels. For each reference drive level there is an optimum microwave input level. Excessive microwave input increases phase noise, temperature drift and decreases IF output.

When checking the diodes in the SPD with a multimeter, be sure the voltage is limited to 2V maximum. While the SPD can be soldered into a circuit by hand, limit the time that each lead is heated to 5 seconds. Also, observe antistatic precautions.

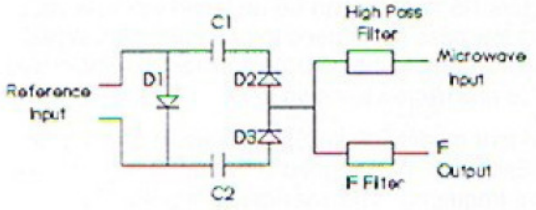


Figure 1

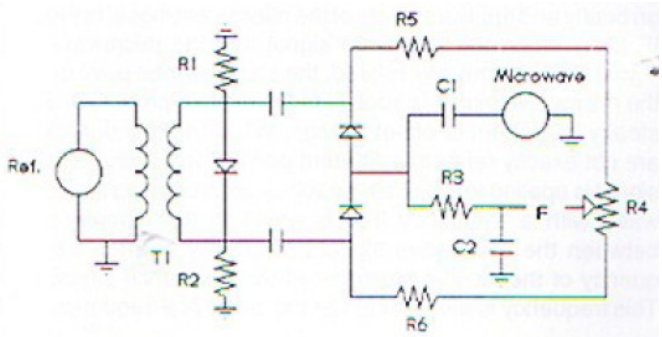


Figure 2

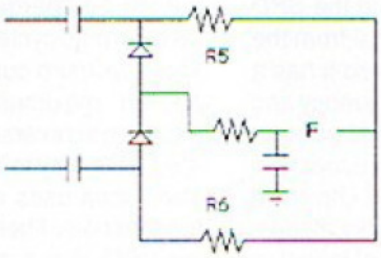


Figure 3

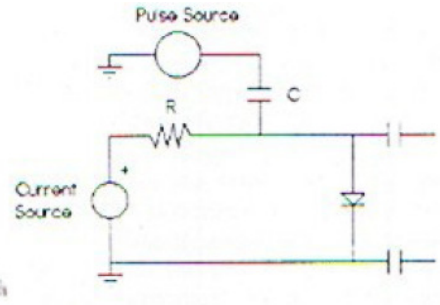


Figure 4

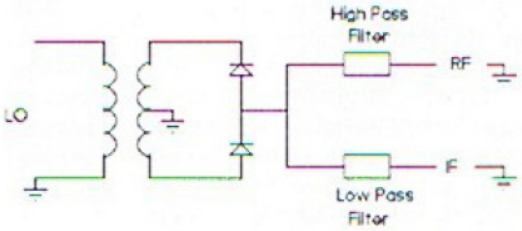


Figure 6

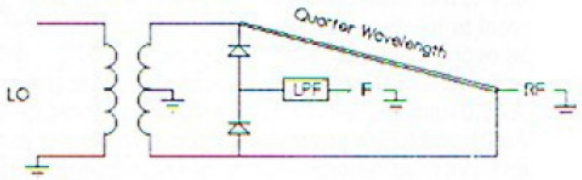
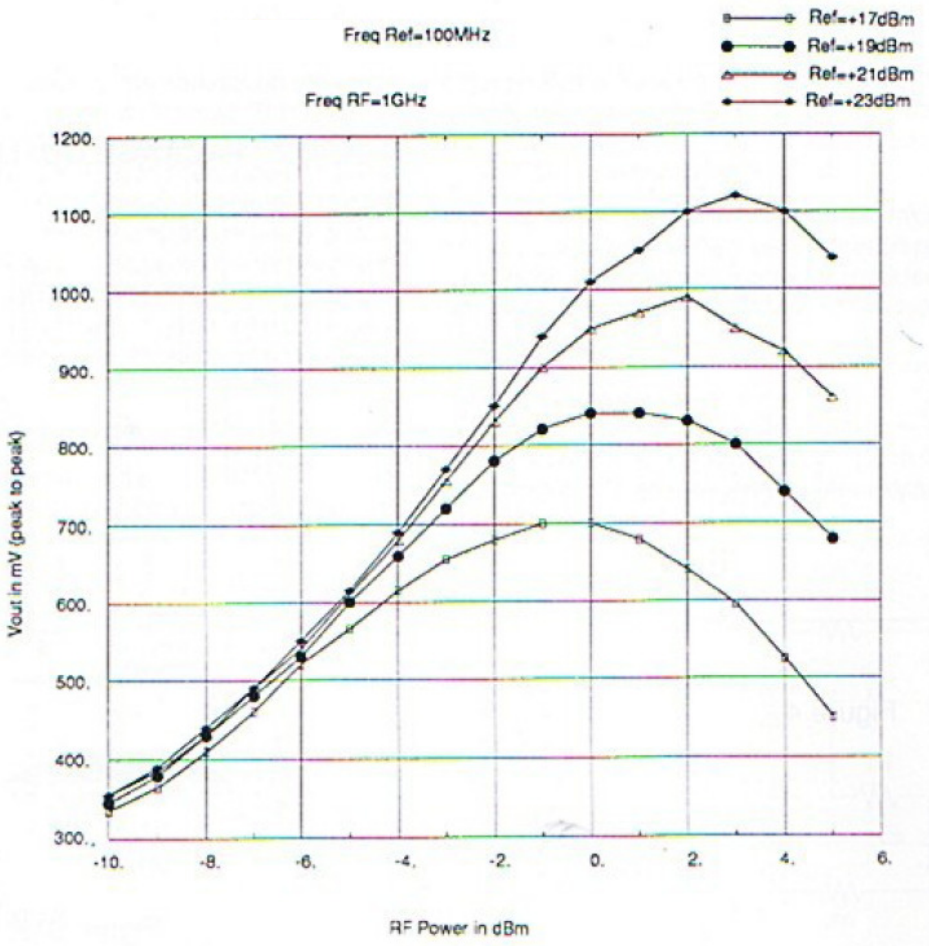


Figure 7

Sampling Phase Detectors



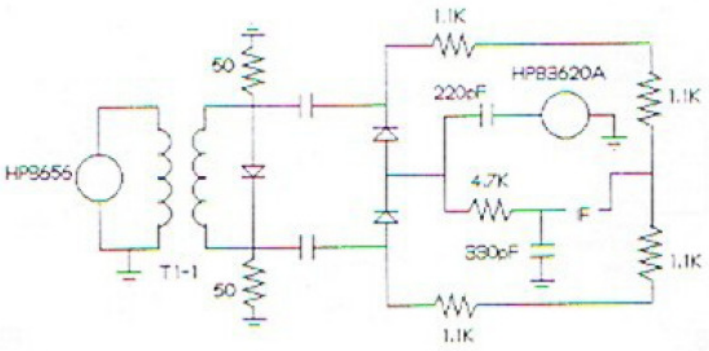
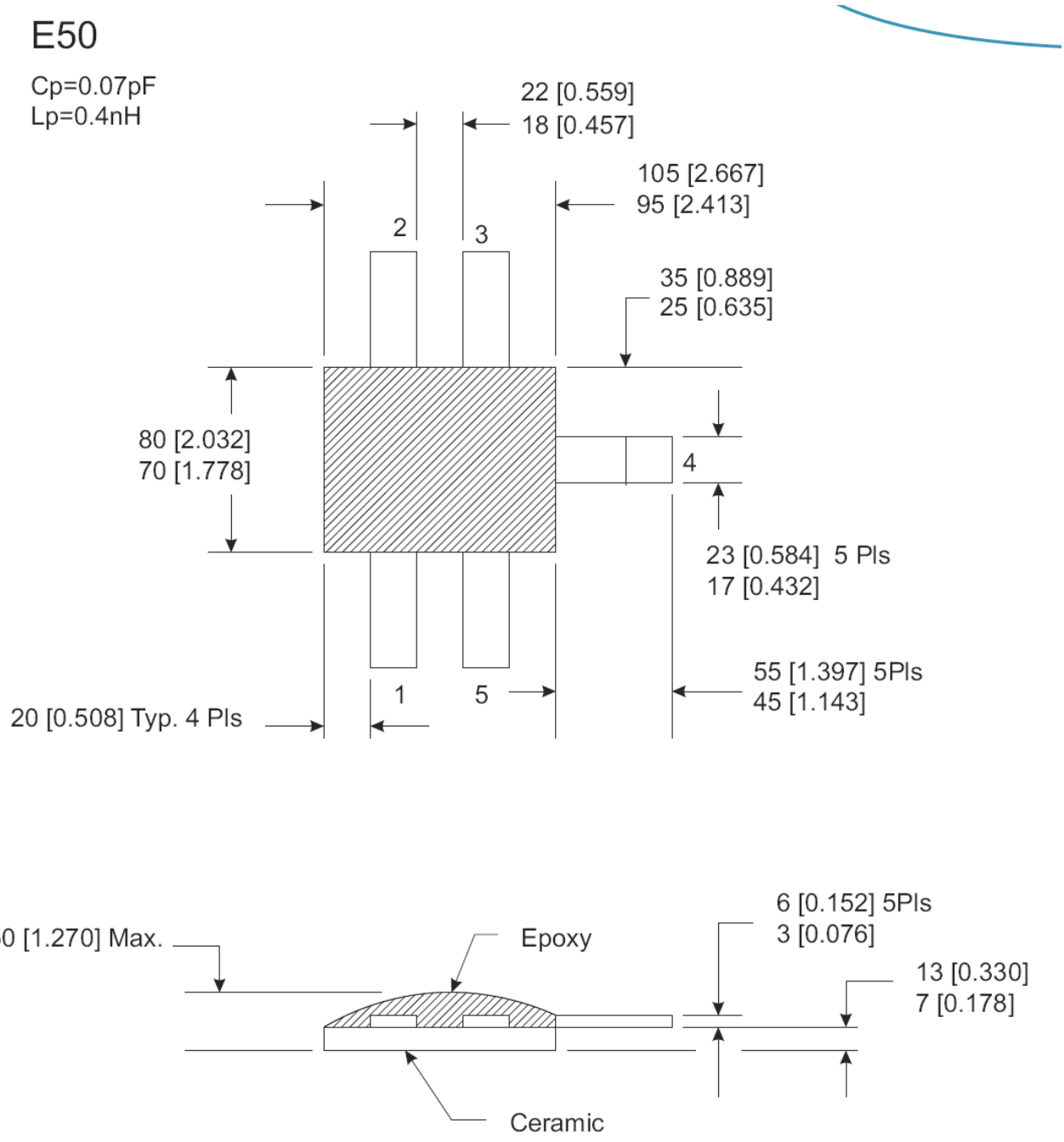


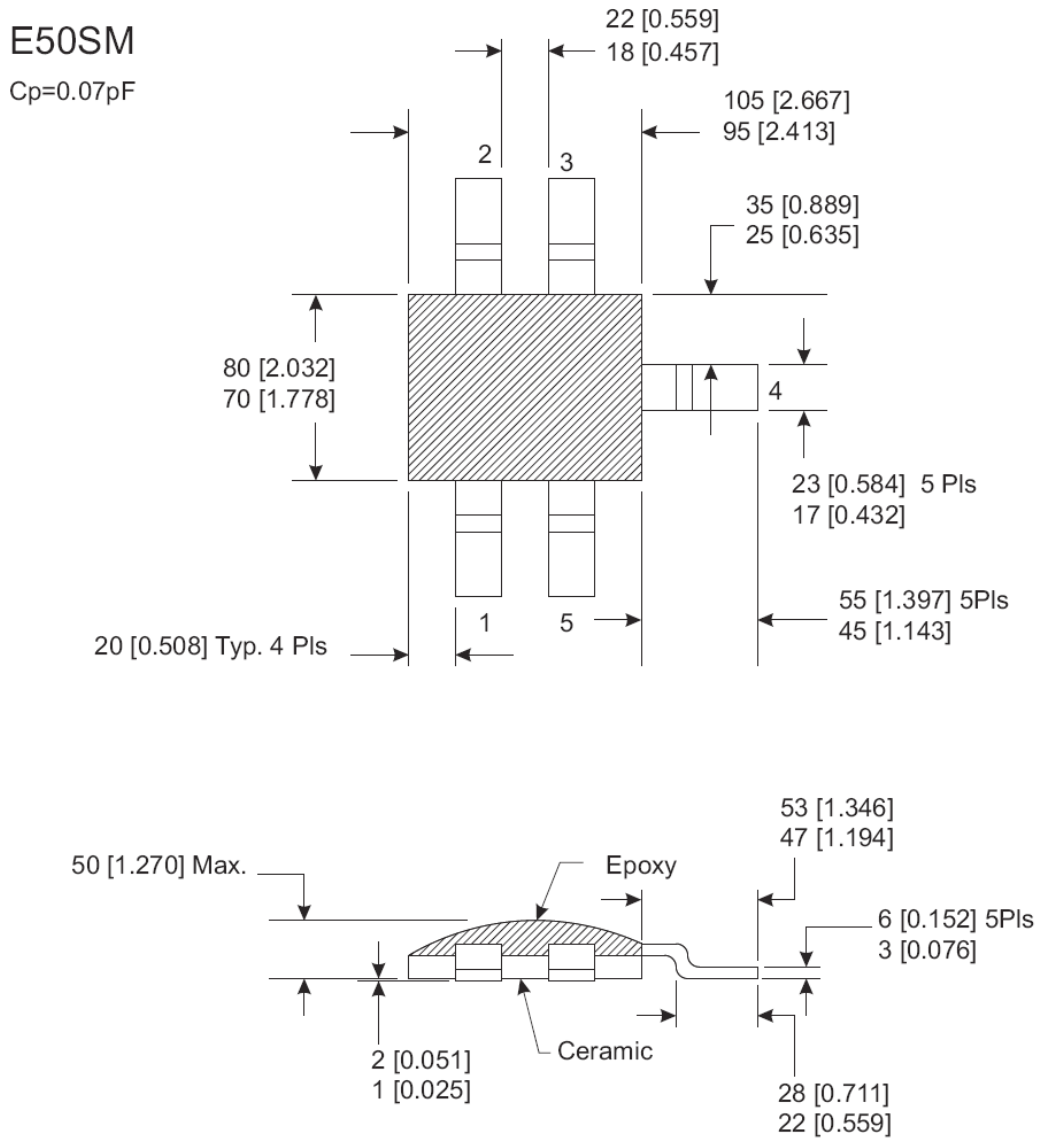
Figure 8

E50 PACKAGE OUTLINE



Dimensions in mils [mm]

E50SM PACKAGE OUTLINE



Dimensions in mils [mm]