

ISL71610M

Radiation Tolerant Passive-Input Digital Isolator

FN9363
Rev.0.00
Nov 8, 2018

The [ISL71610M](#) is a passive-input digital signal isolator with a CMOS output. It has a similar interface but better performance and higher package density than other optocouplers.

The ISL71610M is manufactured with Giant Magnetostrictive (GMR) technology for small size, high speed, and low power. A ceramic/polymer composite barrier provides excellent isolation and an unlimited barrier life. A series external resistor sets the input coil current and a capacitor in parallel with the current-limiting resistor provides improved dynamic performance. This versatile component can be used to replace a variety of optocouplers, functioning over a wide range of data rates, edge speeds, and power supply levels. The device output is compatible with 3.3V and 5V supplies, allowing an interface to controllers without additional level shifting. With the coil energized with a minimum of $\pm 8\text{mA}$ (bidirectional current) the ISL71610M is suitable for single ended and differential drive applications.

The ISL71610M is offered in an 8 Ld 5mmx4mm SOIC package and is fully specified across the military ambient temperature range of -55°C to $+125^\circ\text{C}$.

Applications

- Isolated power
- CAN bus/device net
- Differential line receiver
- Optocoupler replacement
- SPI interface
- RS-485, RS-422, or RS-232

Features

- Barrier Voltage Endurance
 - 2.5kVRMS, for 1 minute, 600Vrms continuous (VDE V 0884-10 certified: file 5022321-4880-0001),
 - 1.5kVDC continuous
 - 500VDC at $43\text{MeV}\cdot\text{cm}^2/\text{mg}$ SEDR
- UL 1577 recognized: file reference E483309
- Up to 100 Mbps data rate
- Flexible inputs with very wide input voltage range (resistor limited current through coil)
- Bipolar current input failsafe output
- No carrier or clock for low EMI emissions and susceptibility
- 3V to 5.5V signaling operation
- Passes NASA low outgassing specifications
- NiPdAu-Ag leadframes (Pb-free, Sn-free)
- Full military temperature range operation
 - $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$
 - $T_J = -55^\circ\text{C}$ to $+150^\circ\text{C}$
- Radiation characterization
 - Low Lose Rate (LDR) ($0.01\text{rad}(\text{Si})/\text{s}$): $30\text{krad}(\text{Si})$
- SEE Characterization
 - No SEB/SEL LET, $V_{DD} = 7\text{V}$: $43\text{MeV}\cdot\text{cm}^2/\text{mg}$

Related Literature

For a full list of related documents, visit our website:

- [ISL71610M](#) product page

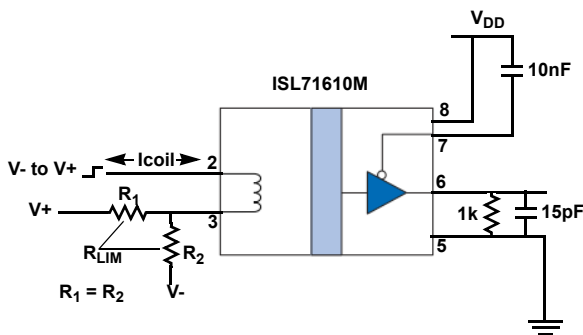


Figure 1. Single-Ended Configuration

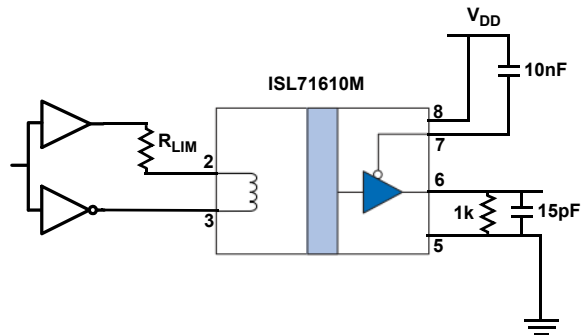


Figure 2. Differential Configuration

Contents

1. Overview	3
1.1 Functional Block Diagram	3
1.2 Ordering Information	3
1.3 Pin Configuration	4
1.4 Pin Descriptions	4
2. Specifications	5
2.1 Absolute Maximum Ratings	5
2.2 Outgas Testing	5
2.3 Thermal Information	5
2.4 Recommended Operating Conditions	6
2.5 Insulation Specifications	6
2.6 Safety and Approvals	6
2.7 Electrical Specifications	7
3. Typical Performance Curves	10
4. Device Information	13
4.1 Coil Polarity	13
4.2 Input Resistor Selection	13
4.3 Single-Ended or Differential Input	13
4.4 Non-Inverting and Inverting Configurations	13
4.5 Boost Capacitor	13
4.6 Dynamic Power Consumption	14
4.7 Power Supply Decoupling	14
4.8 Maintaining Creepage	14
4.9 Electromagnetic Compatibility and Magnetic Field Immunity	14
4.10 Data Rate and Magnetic Field Immunity	14
5. Radiation Tolerance	15
5.1 Total Ionizing Dose (TID) Testing	15
5.2 Single Event Effects Testing	18
6. Revision History	23
7. Package Outline Drawing	24

1. Overview

1.1 Functional Block Diagram

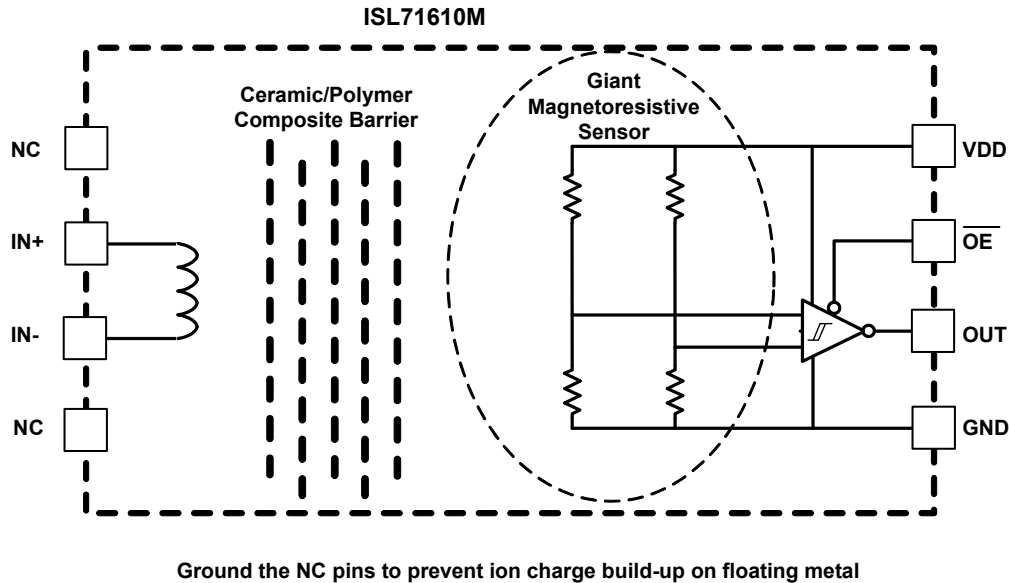


Figure 3. Block Diagram

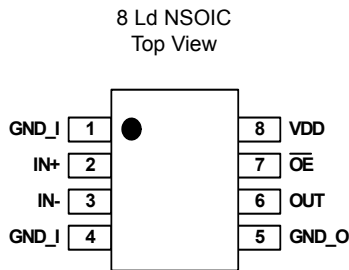
1.2 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temperature Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Package Drawing
ISL71610MBZ	71610 MBZ	-55 to +125	-	8 Ld NSOIC	M8.15G
ISL71610MBZ-T	71610 MBZ	-55 to +125	2.5k	8 Ld NSOIC	M8.15G
ISL71610MBZ-T7A	71610 MBZ	-55 to +125	250	8 Ld NSOIC	M8.15G
ISL71610-710EV1Z	Evaluation Board				

Notes:

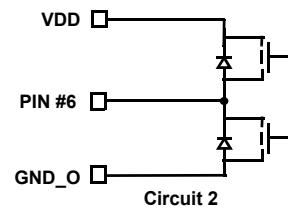
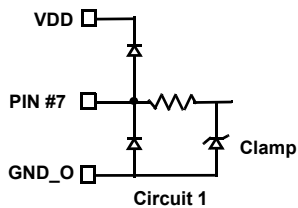
1. Refer to [TB347](#) for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the [ISL71610M](#) device page. For more information about MSL, see [TB363](#).

1.3 Pin Configuration



1.4 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1, 4	GND_I	N/A	No internal connection. Use for input shielding, connect to input side ground
2	IN+	N/A	Coil connection. The voltage applied to IN+ is more negative than IN- to cause the voltage of OUT to switch to V_{OL} (logic low).
3	IN-	N/A	Coil connection. The voltage applied to IN- is more positive than IN+ to cause the voltage of OUT to switch to V_{OL} (logic low).
5	GND_O	N/A	Ground return for VDD
6	OUT	2	Data output. The OUT pin logic high is the zero input current state.
7	\overline{OE}	1	Output enable, active low. Internally pulled low with 100k Ω to enable the output when this pin is not connected.
8	VDD	N/A	Receiver supply voltage



2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VDD	GND - 0.3	GND + 7	V
IN+, IN-	-25	25	mA
OUT, $\overline{\text{OE}}$	GND - 0.3	V _{DD} + 1.5	V
OUT, $\overline{\text{OE}}$	-10	10	mA
Voltage Difference Across the Package (Pins 1, 2, 3, 4 to Pins 5, 6, 7, 8)		500	V
Power Dissipation		675	mW
ESD Rating	Value		Unit
Human Body Model (Tested per AEC-Q100-002)	1.2		kV
Charged Device Model (Tested per AEC-Q100-011)	1.5		kV
Latch-up (Tested per JESD-78E; Class 2, Level A) at +125°C	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Outgas Testing

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Lost (Note 4)	0.06	%
Collected Volatile Condensable Material (Note 4)	<0.01	%
Water Vapor Recovered	0.03	%

Note:

4. Outgassing results meet NASA requirements of total mass loss <1% and collected volatile condensable material of <0.1%.

2.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)
NSOIC Package M8.15G (Notes 5, 6)	60	10

Notes:

5. θ_{JA} is measured with the component soldered to double-sided board; free air.
 6. For Ψ_{JT} characterization parameter, the package top temperature is measured at the top center of the mounted package. See [TB379](#).

Parameter	Minimum	Maximum	Unit
Junction Temperature	-55	+150	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	Refer to TB493		

2.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature	-55	+125	°C
VDD	3	5.5	V
OUT, $\overline{\text{OE}}$	0	V _{DD}	V
OUT	-4	4	mA
Maximum Coil Current	-20	20	mA
Minimum Coil Current to Ensure Correct Output	-8	8	mA

2.5 Insulation Specifications

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Creepage Distance (external)		IPC-2221B	2.54			mm
Total Barrier Thickness (internal)			12	13		μm
Leakage Current		240V _{RMS} , 60Hz		200		nA
Barrier Resistance	R _{IO}	500V _{DC}		>100		TΩ
Barrier Capacitance	C _{IO}	1MHz		7		pF
Comparative Tracking Index	CTI	Per IEC:60112	>175			V
AC High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	V _{IOAC}	+125°C ambient	600			V _{RMS}
DC High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	V _{IODC}	+125°C ambient	1500			V
Barrier Life		100°C, 1000 VRMS, 60% Confidence Level activation energy		44000		Years

2.6 Safety and Approvals

VDE V 0884-10 (VDE V 0884-11 pending) (Basic Isolation; VDE File Number 5022321-4880-0001)

- Working voltage (V_{IORM}): 600V_{RMS} (848V_{PK}); basic insulation; pollution degree 2
- Isolation voltage (V_{ISO}): 2500V_{RMS}
- Transient overvoltage (V_{IOTM}): 4000V_{PK}
- Surge rating: 4000V
- Each part tested at 1590V_{PK} for 1s, 5pC partial discharge limit
- Samples tested at 4000V_{PK} for 60s; then 1358V_{PK} for 10s with 5pC partial discharge limit

Safety-Limiting Values	Symbol	Value	Unit
Safety Rating Ambient Temperature	T _S	+180	°C
Safety Rating Power	P _S	270	mW
Supply Current Safety Rating (Total of Supplies)	I _S	54	mA

UL 1577 (Component Recognition Program File Number E483309)

- Each part tested at 3000V_{RMS} (4240V_{PK}) for 1s; each lot sample tested at 2500V_{RMS} (3530V_{PK}) for 1min

2.7 Electrical Specifications

Unless otherwise noted, $V_{DD} = 3V - 5.5V$; OUT and \overline{OE} are open, VDD is bypassed to GND with a 47nF X7R capacitor; $T_A = T_J = +25^\circ C$. Limits apply across the operating temperature range, $-55^\circ C$ to $+125^\circ C$, unless otherwise stated.

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Input Specifications						
Coil Input Resistance	R_{COIL}	$T = 25^\circ C$	47	85	112	Ω
Coil Input Resistance	R_{COIL}	$T = -55^\circ C$	31	60		Ω
Coil Input Resistance Note 8	R_{COIL}	$T = 125^\circ C$		115	138	Ω
Coil Resistance Temperature Coefficient	TC R_{COIL}			0.2	0.25	Ω/K
Coil Inductance	L_{COIL}			9		nH
DC High Input Threshold (5V)	I_{INH-DC}	Single-ended circuit, $V_{DD} = 4.5V - 5.5V$	0.5	1		mA
DC Low Input Threshold (5V)	I_{INL-DC}	Single-ended circuit, $V_{DD} = 4.5V - 5.5V$		3.5	8	mA
Differential High Input Threshold	$I_{INH-DIFF}$	Differential circuit, $V_{DD} = 3V - 5.5V$, $C_{BOOST} = 0pF$, symmetric reversing input	0.5	1		mA
Differential Low Input Threshold	$I_{INL-DIFF}$	Differential circuit, $V_{DD} = 3V - 5.5V$, $C_{BOOST} = 0pF$, symmetric reversing input		3.5	8	mA
Failsafe High Input Current (5V)	$I_{FS-HIGH}$	Single-ended circuit, $V_{DD} = 4.5V - 5.5V$	-25		0.5	mA
Failsafe Low Input Current (5V)	I_{FS-LOW}	Single-ended circuit, $V_{DD} = 4.5V - 5.5V$	5		25	mA
Input Signal Rise and Fall Times	t_{IR}, t_{IF}				1	μs
Common-Mode Transient Immunity	$ CM_H , CM_L $	$V_{TRANSIENT} = 300V_{PEAK}$	15	20		kV/ μs
5V Electrical Specifications ($V_{DD} = 4.5V - 5.5V$; $T = -55^\circ C$ to $+125^\circ C$ unless otherwise stated)						
5V Quiescent Supply Current Note 8	I_{DDQ}	IN+ = IN- = open		2	3	mA
Logic High Output Voltage	V_{OH}	$V_{DD} = 5V$, OUT = 20 μA	4.9	5		V
		$V_{DD} = 5V$, OUT = 4mA	4.0	4.8		V
Logic High Output Drive Current Note 8	I_{OH}			-10	-7	mA
Logic Low Output Voltage	V_{OL}	$V_{DD} = 5V$, OUT = -20 μA		0	0.1	V
		$V_{DD} = 5V$, OUT = -4mA		0.2	0.8	V
Logic Low Output Drive Current Note 8	I_{OL}		7	10		mA
Output Disable	V_{OE}			2.7		V
5 V Switching Specifications ($V_{DD} = 4.5V - 5.5V$; $T = -55^\circ C$ to $+125^\circ C$ unless otherwise stated)						
Data Rate		Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$			100	Mbps
Minimum Pulse-Width	PW	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$	10			ns
Propagation Delay Input to Output (High-to-Low) Note 8	t_{PHL}	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$		8	15	ns
Propagation Delay Input to Output (Low-to-High) Note 8	t_{PLH}	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$		8	15	ns
Average Propagation Delay Drift	t_{PDD}	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$		10		ps/ $^\circ C$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $ Note 8	PWD	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$		3	6	ns
Pulse Jitter	t_j	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$		100		ps

Unless otherwise noted, $V_{DD} = 3V - 5.5V$; OUT and \overline{OE} are open, VDD is bypassed to GND with a 47nF X7R capacitor; $T_A = T_J = +25^\circ C$. Limits apply across the operating temperature range, $-55^\circ C$ to $+125^\circ C$, unless otherwise stated. (Continued)

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Propagation Delay Skew	t_{PSK}	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$	-2		2	ns
Propagation Delay Enable to Output (High-to-High Impedance)	t_{PHZ}	$C_L = 15pF$	-	3	7	ns
Propagation Delay Enable to Output (Low-to-High Impedance)	t_{PLZ}	$C_L = 15pF$	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-High)	t_{PZH}	$C_L = 15pF$	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-Low)	t_{PZL}	$C_L = 15pF$	-	3	7	ns
Output Rise Time (10–90%)	t_R	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$		2	4	ns
Output Fall Time (10–90%)	t_F	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$		2	4	ns
3.3V Electrical Specifications ($V_{DD} = 3V - 3.6V$; $T = -55^\circ C - 125^\circ C$ unless otherwise stated)						
3.3V Quiescent Supply Current	I_{DDQ}	IN+ = IN- = open		1.3	2	mA
Logic High Output Voltage	V_{OH}	$V_{DD} = 3.3V$, OUT = 20 μ A	3.2	3.3		V
Logic High Output Voltage	V_{OH}	$V_{DD} = 3.3V$, OUT = 4mA	3.0	3.1		V
Logic High Output Drive Current Note 8	I_{OH}			-10	-7	mA
Logic Low Output Voltage	V_{OL}	$V_{DD} = 3.3V$, OUT = -20 μ A		0	0.1	V
Logic Low Output Voltage	V_{OL}	$V_{DD} = 3.3V$, OUT = -4mA		0.2	0.8	V
Logic Low Output Drive Current Note 8	I_{OL}		7	10		mA
Output Disable	V_{OE}			1.6		V
3.3V Switching Specifications ($V_{DD} = 3V - 3.6V$; $T = -55^\circ C - 125^\circ C$ unless otherwise stated)						
Data Rate		Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$			100	Mbps
Minimum Pulse Width	PW	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$	10			ns
Propagation Delay Input to Output (High-to-Low) Note 8	t_{PHL}	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$		12	18	ns
Propagation Delay Input to Output (Low-to-High) Note 8	t_{PLH}	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$		12	18	ns
Average Propagation Delay Drift	t_{PDD}	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$		10		ps/ $^\circ C$
Pulse Width Distortion $t_{PHL} - t_{PLH}$ Note 8	PWD	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$		3	6	ns
Propagation Delay Skew	t_{PSK}	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$	-2		2	ns
Propagation Delay Enable to Output (High-to-High Impedance)	t_{PHZ}	$C_L = 15pF$	-	3	7	ns
Propagation Delay Enable to Output (Low-to-High Impedance)	t_{PLZ}	$C_L = 15pF$	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-High)	t_{PZH}	$C_L = 15pF$	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-Low)	t_{PZL}	$C_L = 15pF$	-	3	7	ns

Unless otherwise noted, $V_{DD} = 3V - 5.5V$; OUT and \overline{OE} are open, VDD is bypassed to GND with a 47nF X7R capacitor; $T_A = T_J = +25^\circ C$. Limits apply across the operating temperature range, $-55^\circ C$ to $+125^\circ C$, unless otherwise stated. **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Output Rise Time (10–90%)	t_R	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$		3	5	ns
Output Fall Time (10–90%)	t_F	Single-ended circuit, $t_{IR} = t_{IF} = 3ns$, $C_{BOOST} = 16pF$, $R_{OUT} = 1k\Omega$, $C_{OUT} = 16pF$		3	5	ns

Note:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
8. Parameter tested in production.

3. Typical Performance Curves

$V_{DD} = 5V$, $T_A = +25^\circ C$, unless otherwise specified.

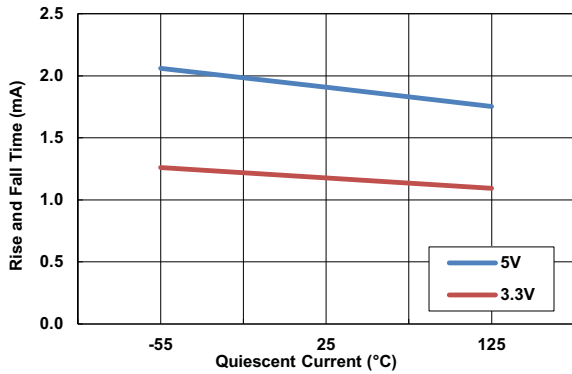


Figure 4. Quiescent Current vs Temperature

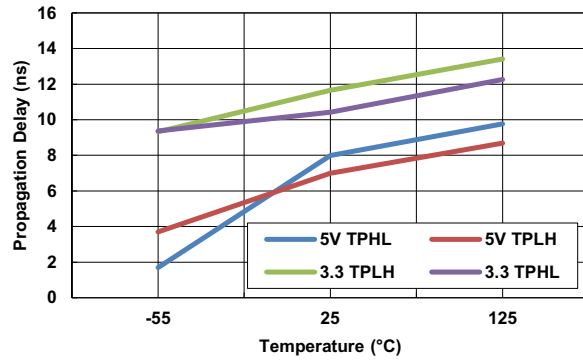


Figure 5. Propagation Delay vs Temperature, Voltage

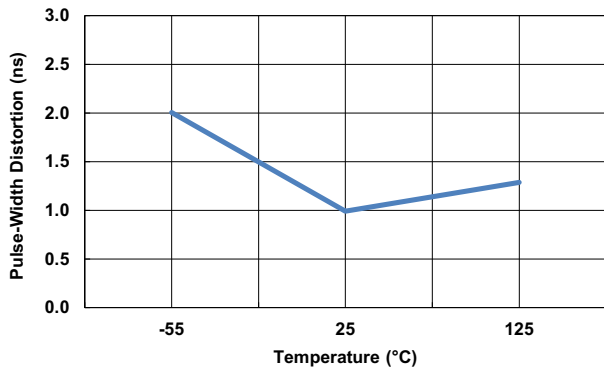


Figure 6. Pulse-Width Distortion vs Temperature

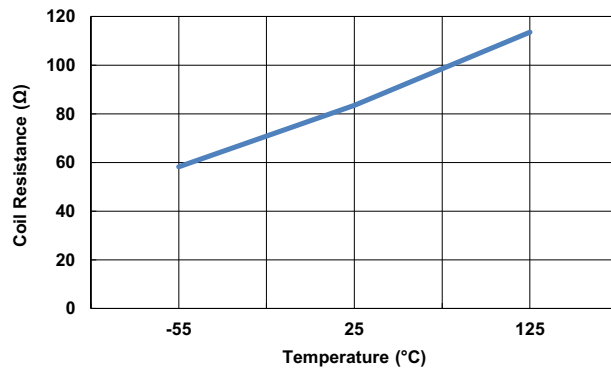


Figure 7. Coil Resistance vs Temperature

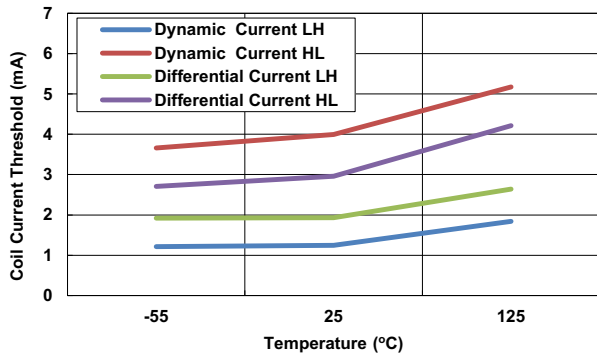


Figure 8. Coil Current Threshold vs Temperature, Voltage

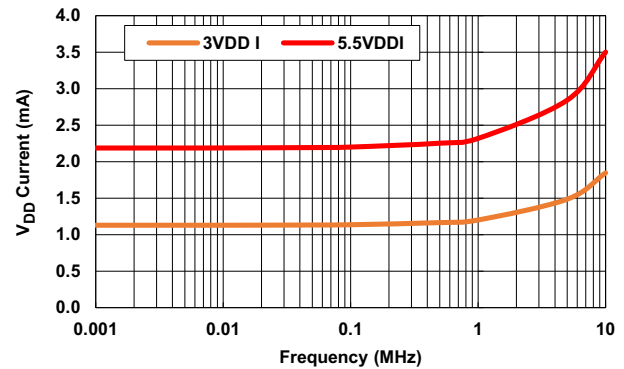


Figure 9. V_{DD} Current vs Frequency, Voltage, 0 load, 50% Duty Cycle

$V_{DD} = 5V$, $T_A = +25^\circ C$, unless otherwise specified. (Continued)

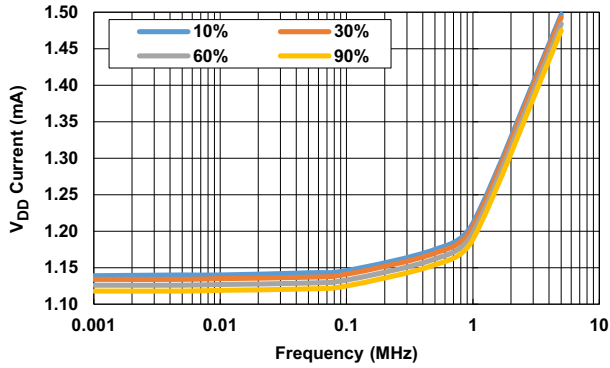


Figure 10. 3V V_{DD} Current vs Frequency, Duty Cycle, 0 load

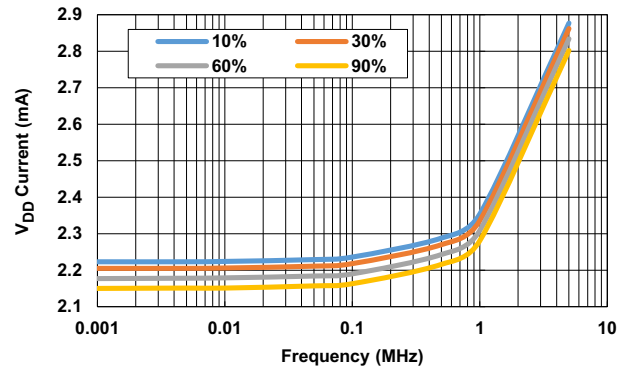


Figure 11. 5.5V V_{DD} Current vs Frequency, Duty Cycle, 0 load

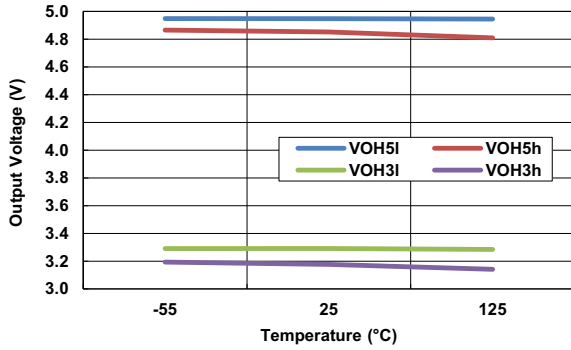


Figure 12. Output High Voltage for 5V and 3.3V with I_{out} of $20\mu A$ and 4mA

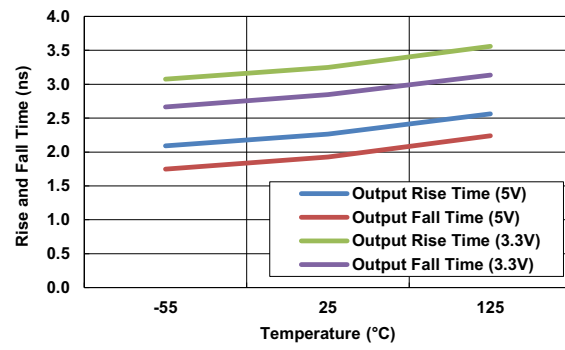


Figure 13. Rise and Fall Time vs Voltage and Temperature

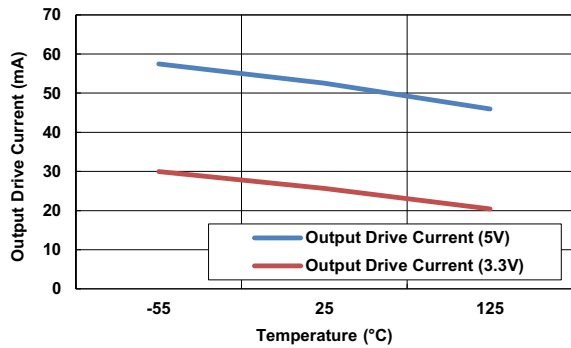


Figure 14. Output Drive Current Capability vs Temperature and Voltage

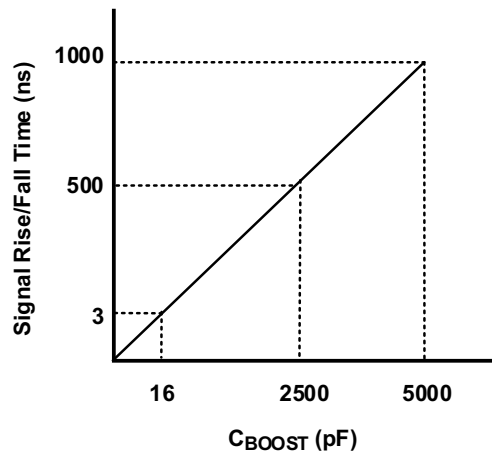


Figure 15. Boost Capacitor (C_{BOOST}) Selector Guide

$V_{DD} = 5V$, $T_A = +25^\circ C$, unless otherwise specified. VRlimit trace shows the timing of the coil current through the current limiting resistor and coil as a voltage across the resistor and coil, coil current rise/fall time $\sim 20ns$, V_{OUT} rise/fall time $\sim 10ns$.

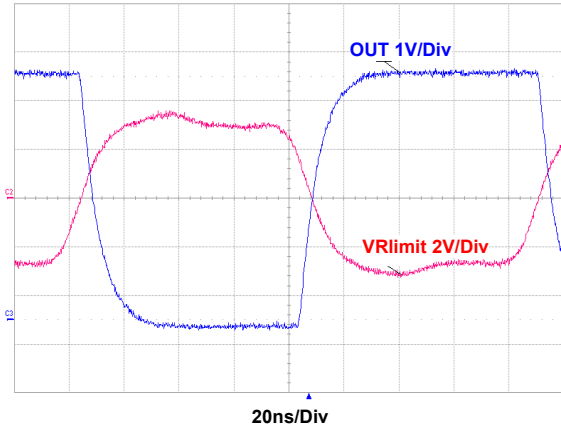


Figure 16. Switching, Coil Current $\sim \pm 8mA$, $C_{BOOST} = 15pF$, $C_{OUT} = 15pF$, $V_{DD} = 5V$

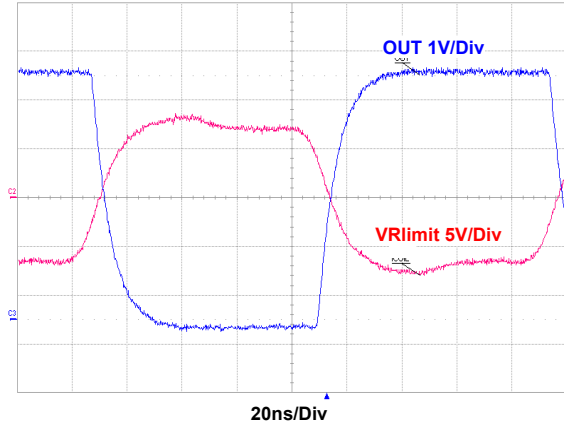


Figure 17. Switching, Coil Current $\sim \pm 18mA$, $C_{BOOST} = 15pF$, $C_{OUT} = 15pF$, $V_{DD} = 5V$

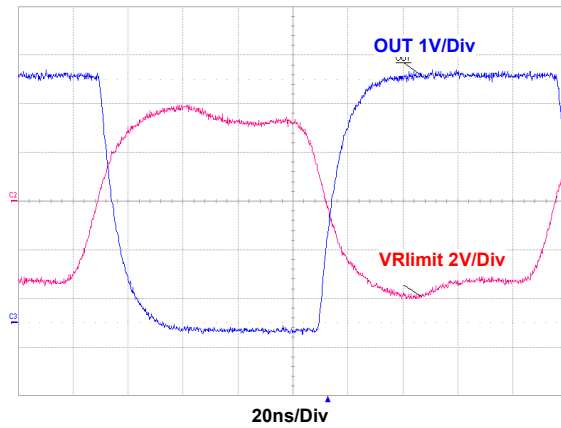


Figure 18. Switching, Coil Current $\sim \pm 8mA$, $C_{BOOST} = 5pF$, $C_{OUT} = 15pF$, $V_{DD} = 5V$

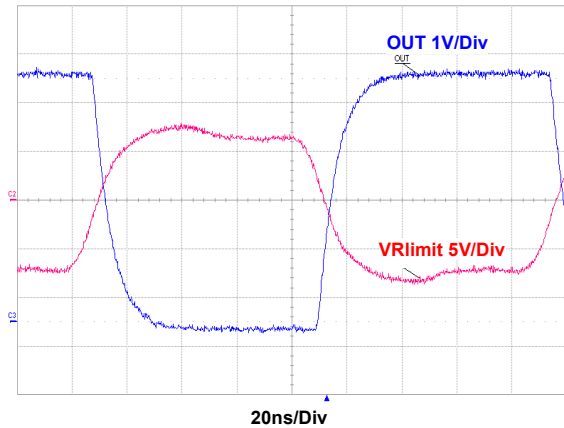


Figure 19. Switching, Coil Current $\sim \pm 18mA$, $C_{BOOST} = 5pF$, $C_{OUT} = 15pF$, $V_{DD} = 5V$

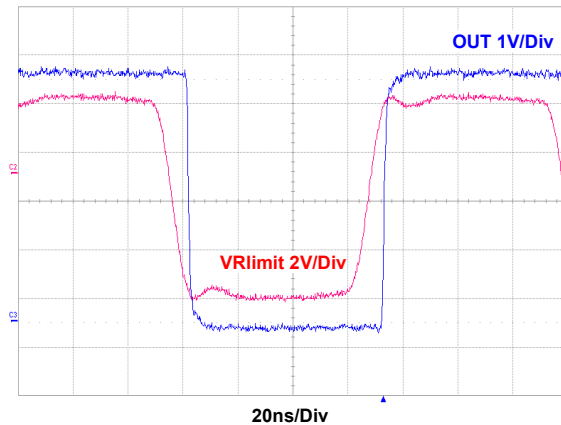


Figure 20. Non Inverting Configuration, Switching Coil Current $\sim \pm 10mA$, $C_{BOOST} = 5pF$, $C_{OUT} = 15pF$, $V_{DD} = 5V$

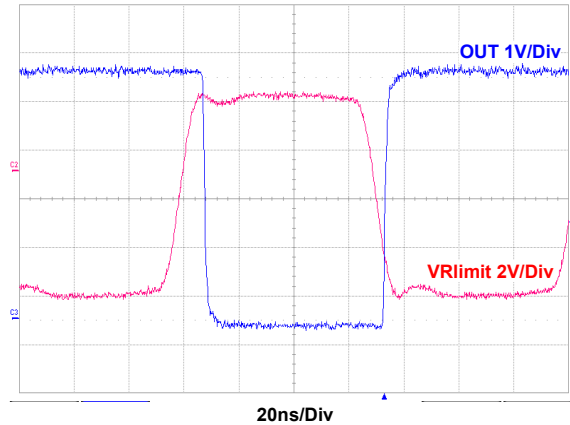


Figure 21. Inverting Configuration, Switching, Coil Current $\sim \pm 10mA$, $C_{BOOST} = 5pF$, $C_{OUT} = 15pF$, $V_{DD} = 5V$

4. Device Information

The ISL71610M isolator is a passive input current mode device. Changes in current flow into the input coil result in logic state changes at the output.

4.1 Coil Polarity

The ISL71610M switches to logic low if current flows from the IN- pin to the IN+ pin. Note that the designations “IN-” and “IN+” refer to logic levels, not current flow. Positive current values means conventional current flows into the IN- input. To ensure an output state in an ion environment the coil must be energized in either direction and must not be in a zero current condition. [Figures 16](#) through [21](#) illustrate the bidirectional current drive waveforms.

4.2 Input Resistor Selection

A series resistor sets the coil input current. There is no limit to the input voltage amplitude because there are no semiconductor input structures. The minimum current amplitude for an assured output state across the voltage range is $\pm 8\text{mA}$. A “boost capacitor” creates current reversals at edge transitions, reducing the input logic low threshold current to the differential level of 5mA . For a 25°C 8mA coil current, a typical resistor value for 3.3V signaling is 324Ω and a typical value for 5V signaling is 511Ω based on an 85Ω coil resistance. These values are approximate and should be adjusted for temperature or other application specifics. Consult the coil resistance specification and temperature coefficient graph for further information and guidance. If the expected temperature range is large, 1% tolerance resistors may provide additional design margin.

4.3 Single-Ended or Differential Input

The ISL71610M can be run with single-ended or differential inputs. In differential mode, the current naturally flows through the coil in both directions without a boost capacitor, although the capacitor can still be used for increased external field immunity or improved pulse-width distortion. Due to SEE testing results, the single-ended mode of operation should be implemented with $\pm 8\text{mA}$ min of coil current as shown in [Figure 1 on page 1](#). Using a ground referenced single-ended configuration where there is 0 coil current can result in output state changes, see [Figure 34 on page 19](#).

An advantage over optocouplers and other high-speed couplers in differential mode is that no reverse bias protection for the input structure is required for a differential signal.

One of the more common applications is for an isolated differential line receiver. For example, RS-485 can drive an ISL71610M directly for a fraction of the cost of an isolated RS-485 node.

4.4 Non-Inverting and Inverting Configurations

ISL71610M can be configured in non-inverting and inverting configurations, each is defined by the direction of current flow through the coil. In the non-inverting configuration current flows through the coil from the IN- side to the IN+ side. The +IN is at a higher voltage potential than the -IN.

4.5 Boost Capacitor

The boost capacitor in parallel with the current-limiting resistor boosts the instantaneous coil current at the signal transition. This ensures switching and reduces propagation delay and reduces pulse-width distortion.

Select the value of the boost capacitor based on the rise and fall times of the signal driving the inputs. The instantaneous boost capacitor current is proportional to input edge speeds ($C * dV/dt$). Select a capacitor value based on the rise and fall times of the input signal to be isolated that provides approximately 20mA of additional “boost” current. For high-speed logic signals ($t_R, t_F < 10\text{ns}$), a 16pF capacitor is recommended. The capacitor value is generally not critical; if in doubt, choose a higher value. See [Figure 16 on page 12](#).

4.6 Dynamic Power Consumption

Power consumption is proportional to duty cycle, not data rate. The use of NRZ coding minimizes power dissipation because no additional power is consumed when the output is in the high state. In differential mode, where the logic high condition may still require a current to be forced through the coil, power consumption is higher than a typical NRZ single-ended configuration. See [Figures 14](#) through [16](#) for typical power consumption performance.

4.7 Power Supply Decoupling

A 47nF low-ESR ceramic capacitor is recommended to decouple the power supply. Place the capacitor as close as possible to the VDD pin.

4.8 Maintaining Creepage

Creepage distances are often critical in isolated circuits. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance.

4.9 Electromagnetic Compatibility and Magnetic Field Immunity

Because the ISL71610M is completely static, it has the lowest emitted noise of any non-optical isolators. The ISL71610M operates by imposing a magnetic field on a GMR sensor, which translates the change in field into a change in logic state. A magnetic shield and a Wheatstone Bridge configuration provide good immunity to external magnetic fields. Immunity to external magnetic fields can be enhanced by proper orientation of the device with respect to the field direction, the use of differential signaling, and boost capacitors.

4.9.1 Orientation of the Device with Respect to the Field Direction

An applied field into the pin edges of the package is the worst case for magnetic immunity. In this case, the external field is in the same direction as the applied internal field. In one direction it tends to help switching; in the other it hinders switching. This can cause unpredictable operation.

An applied field into the pin-less edges of the package has considerably less effect and results in higher magnetic immunity.

4.9.2 Differential Signaling and Boost Capacitors

Regardless of orientation, driving the coil differentially improves magnetic immunity. This is because the logic high state is driven by an applied field instead of zero field, as is the case with single-ended operation. The higher the coil current, the higher the internal field and the higher the immunity to external fields. Optimal magnetic immunity is achieved by adding the boost capacitor.

4.10 Data Rate and Magnetic Field Immunity

It is easier to disrupt an isolated DC signal with an external magnetic field than it is to disrupt an isolated AC signal. Similarly, a DC magnetic field has a greater effect on the device than an AC magnetic field of the same effective magnitude. For example, signals with pulses longer than 100 μ s are more susceptible to magnetic fields than shorter pulse widths.

5. Radiation Tolerance

The ISL71610M isolator is a radiation tolerant device for commercial space applications, Low Earth Orbits (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device's response to Total Ionizing Dose (TID) radiation effects and Single Event Effects (SEE) has been measured, characterized, and reported in the preceding sections. However, TID performance is not guaranteed through radiation acceptance testing, nor is the characterized SEE performance guaranteed.

5.1 Total Ionizing Dose (TID) Testing

Total dose testing of the ISL71610MBZ proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 32 samples irradiated at a 5.5V bias, as shown in [Table 1](#), and 16 samples irradiated with all pins grounded (unbiased). Three control units were used. The bias configuration is shown in [Figure 31 on page 17](#). Samples of the ISL71610MBZ were packaged in the production 8 Ld plastic NSOIC, Package Outline Drawing (POD) M8.15G. The samples were screened to datasheet limits at +125°C temperature only before irradiation.

Total dose irradiations were performed using a Hopewell Designs N40 panoramic vault-type low dose rate 60Co irradiator located in the Renesas Palm Bay, Florida facility. The dose rate was < 10mrad(Si)/s). PbAl spectrum hardening filters were used to shield the test board and devices under test against low energy secondary gamma radiation.

Down-points for the testing were 0krad(Si), 10krad(Si), 20krad(Si), and 30krad(Si). All electrical testing was performed outside the irradiator using production Automated Test Equipment (ATE) with data logging of all parameters at each down-point. All down-point electrical testing was performed at +25°C temperature.

5.1.1 Results

[Table 1](#) summarizes the attributes data. Note that “Bin 1” indicates a device that passes all datasheet specification limits.

Table 1. ISL71610M Total Dose Test Attributes Data

Bias	Sample Size	Down Point	Bin 1	Rejects
Figure 31	32	Pre-rad	32	
		10krad(Si)	32	0
		20krad(Si)	32	0
		30krad(Si)	32	0
Grounded	16	Pre-rad	16	
		10krad(Si)	16	0
		20krad(Si)	16	0
		30krad(Si)	16	0

The plots in [Figures 22](#) through [30](#) show data for key parameters at all down points. The plots show the average as a function of total dose for each of the irradiation conditions; we chose to use the average because of the relatively large sample sizes. All parts showed excellent stability over irradiation.

[Table 2 on page 17](#) shows the average of some of these key parameters with respect to total dose in tabular form.

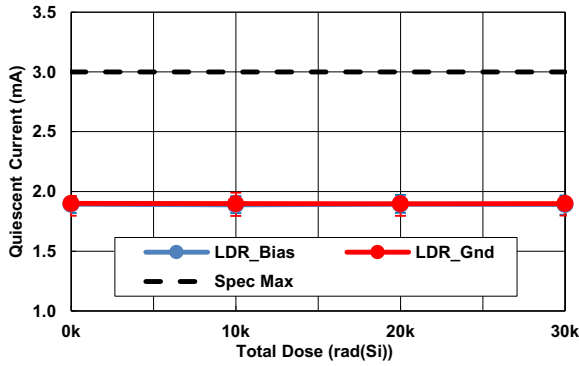


Figure 22. 5V Quiescent Supply Current vs TID

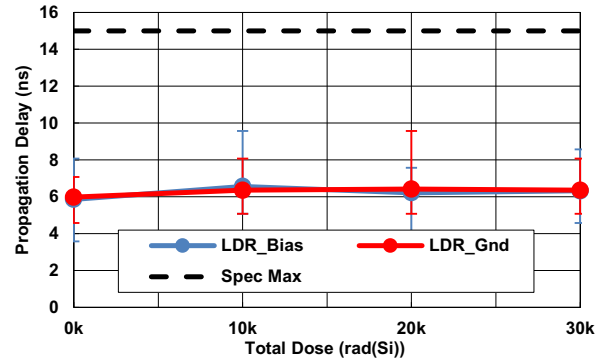


Figure 23. Propagation Delay High-to-Low vs TID

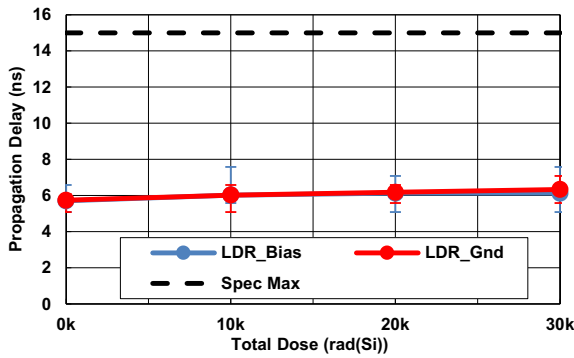


Figure 24. Propagation Delay Low-to-High vs TID

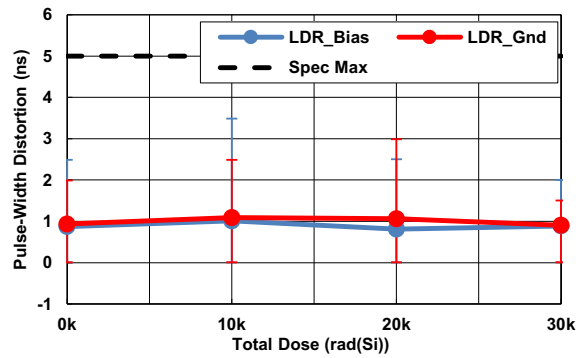


Figure 25. Pulse-Width Distortion vs TID

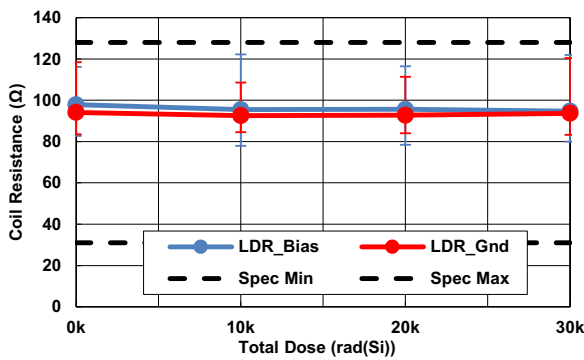


Figure 26. Coil Resistance vs TID

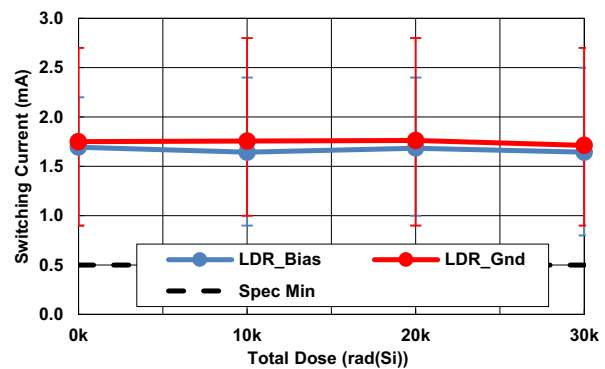


Figure 27. 3V Low-to-High Switching Current vs TID

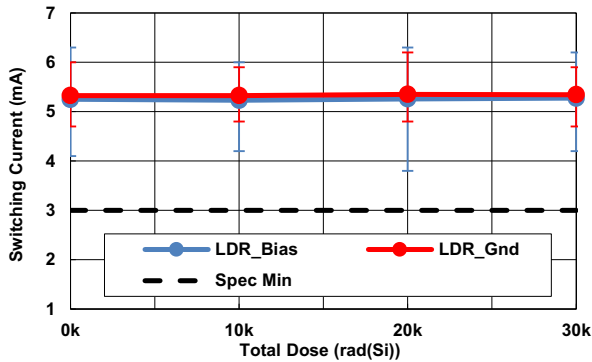


Figure 28. 3V High-to-Low Switching Current vs TID

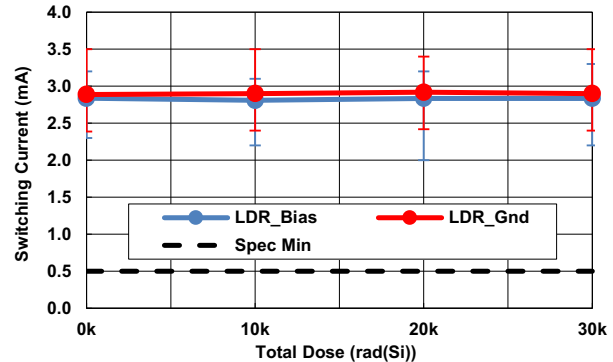


Figure 29. 5V Low-to-High Switching Current vs TID

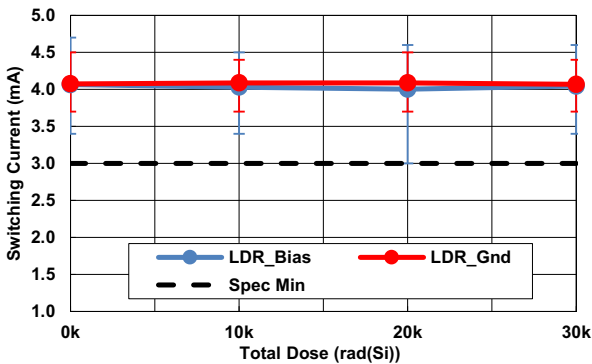


Figure 30. 5V High-to-Low Switching Current vs TID

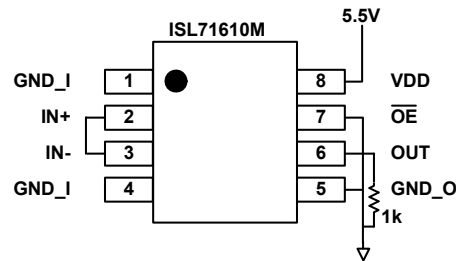


Figure 31. TID Biased Configuration

5.1.2 Conclusion

ATE characterization testing showed no rejects to the datasheet limits at all down points. No differences between biased and unbiased irradiation were noted and the part is not considered bias sensitive.

Table 2. ISL71610M Response of Selected Key Parameters vs TID

Parameter	Bias	0krad(Si)	10krad(Si)	20krad(Si)	30krad(Si)	Unit
5V Quiescent Supply Current	Biased	1.893105	1.888049	1.892899	1.890288	mA
	Grounded	1.9003	1.897326	1.896655	1.898356	
Propagation Delay Input to Output (High-to-Low)	Biased	5.858396	6.560396	6.217196	6.326396	ns
	Grounded	5.983196	6.357596	6.419997	6.357596	
Propagation Delay Input to Output (Low-to-High)	Biased	5.709593	6.021594	6.130794	6.130744	ns
	Grounded	5.740793	6.021295	6.177396	6.333395	
Pulse-Width Distortion	Biased	0.8736	1.011751	0.811188	0.889199	ns
	Grounded	0.935999	1.0911	1.0617	0.904802	
Coil Resistance	Biased	97.88696	95.43535	95.59083	94.73875	Ω
	Grounded	94.08835	92.5607	92.76359	93.72113	

5.2 Single Event Effects Testing

The intense heavy ion environment encountered in space applications can cause a variety of Single Event Effects (SEE). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. The following is a summary of the SEE testing of the ISL71610M.

5.2.1 SEE Test Facility

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility. This facility is coupled to a K500 superconducting cyclotron, which is capable of generating a wide range of test particles with the various energy, flux, and fluence level needed for advanced radiation testing.

5.2.2 Scope of the ISL71610M SEE Testing

The ISL71610M is a single channel, passive input, digital isolator with a CMOS compatible output packaged in an 8 Ld NSOIC package. The testing described here was undertaken for a preliminary evaluation of the ISL71610M for use in space applications. Both destructive Single Event Dielectric Rupture (SEDR) of the barrier isolation and non-destructive Single Event Transients (SET) were tested. In addition, destructive Single Event Burnout (SEB) and Single Event Latch-Up (SEL) of the CMOS circuitry were tested.

5.2.3 Testing Set Up

The plastic packages were opened chemically to expose the die surface so that SEE testing could be accomplished. Care had to be observed to ensure that the plastic was opened but that the isolation barrier was not compromised. This took a bit of trial and error, but a process to open the parts was found. When opened, the barrier isolation was degraded by free air breakdown to about 750VDC.

Four parts were mounted close together on boards for simultaneous irradiation. For the barrier SEDR testing the pins on either side of the barrier were all shorted together (1-4 on one side and 5-8 on the other side) so that a high voltage could be applied across the isolation barrier. For SEB and SEL testing the parts were powered with various voltages while irradiating. For both forms of destructive SEE the parts were heated to +125°C. For the SET testing the parts were at +25°C and biased with either 3.0V or 5.5V supplies with static inputs of both states tested.

5.2.4 Isolation Barrier SEDR Testing

The ISL71610M barrier isolation SEDR was tested by biasing the four parts with 200V to 500V in 50V increments while irradiating with normal incidence silver (Ag) for a surface LET of 43MeV·cm²/mg to a fluence of 1x10⁷ ion/cm² at each of the seven voltages. The four parts were heated to +125°C for the testing. The leakage current across the barrier of each part was measured before and after each irradiation to assess the change. The leakages all measured below 75nA both before and after irradiation. No leakage changed by more than 50% as a result of the irradiation being observed. The isolation barrier is rated to 500V over the entire operational envelope.

5.2.5 SEB and SEL Testing

For this testing the isolation barrier voltage was set to 0V and the four parts were powered with supply voltages of 5.5V, 6.0V, 6.5V, and 7.0V.

The parts were heated to +125°C during the testing. Before and after each irradiation to 1x10⁷ ion/cm² with normal incidence silver for silver (Ag) for a surface LET of 43MeV·cm²/mg the supply currents and the output voltages were measured at a V_{DD} of 5.0V at both input states to exercise both output conditions. During irradiation the input had a 500kHz signal applied (0-5mA) and none of the monitored values changed significantly (more than 1%) during the irradiations establishing 7V as the maximum V_{DD} voltage.

5.2.6 SET Testing

The ISL71610M was tested for qualification of Single Events Transients (SET) on October 16, 2018. The testing was done at TAMU's Cyclotron Institute. The SET test plan was constructed based on results from preliminary testing of the NVE IL610, which is the same base part. The results of most interest for the preliminary testing (June 2017 and December 2017) were the two forms of observed SET for the IL610 at the LET level of $43\text{MeV}\cdot\text{cm}^2/\text{mg}$. The first form was a spike SET where the output had a transition toward the opposite state for a very short time, less than 50ns, (Figures 32 and 33). The second type of SET previously observed was a state change SET. Figure 34 shows where the output transitioned to the opposite state and stayed there until another event triggered it back again.

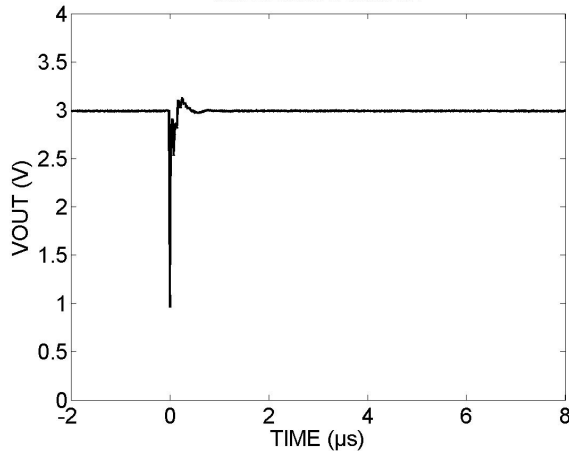


Figure 32. 0mA in Coil, Output High, $V_{DD} = 3.0\text{V}$

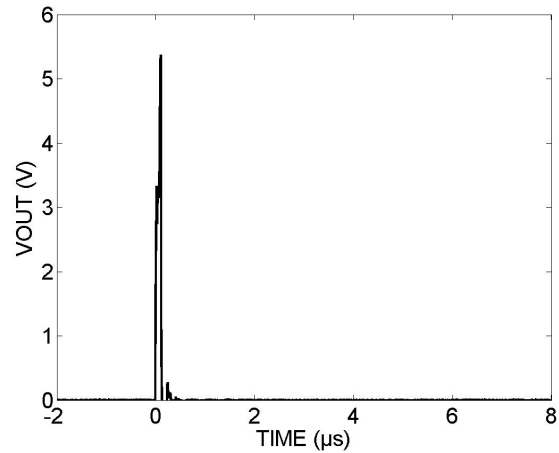


Figure 33. 5mA Through Coil, Output Low, $V_{DD} = 5.5\text{V}$

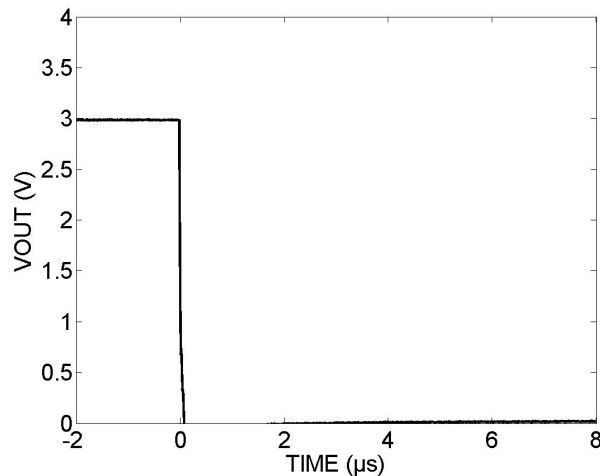


Figure 34. 0mA in Coil, Output Latched Low, $V_{DD} = 3.0\text{V}$

The state change events were always when the coil current was 0A and the V_{DD} was at 3.00V. The pertinent SET counts from the previous testing appear in [Table 3](#).

Table 3. SET Type Counts for Previous Testing of the ISL71610M Done in June 2017 and December 2017

Date	V_{DD} (V)	IN- (mA)	Spike SET Counts by DUT					State Change SET by DUT				
			1	2	3	4	Total	1	2	3	4	Total
6-17	3.0	0	11	5	10	0	26	0	19	0	32	51
	3.0	5	1	0	0	0	1	0	0	0	0	0
	5.5	5	10	0	18	0	28	0	0	0	0	0
	5.5	0	0	0	0	0	0	0	0	0	0	0
12-17	3.0	0	0	14	0	9	23	20	0	22	0	42
	3.0	5	0	8	0	0	8	0	0	0	0	0
	5.5	5	0	6	0	0	6	0	0	0	0	0
	5.5	0	6	5	13	0	24	0	0	0	0	0

In addition to the specific conditions associated with the state changes, it should be noted that only four of the eight units tested exhibited the state change SETs. Another important observation is that the parts that exhibited the state change events did not exhibit any state changes when a current was applied to the input. Although the current was always a positive current (to give a low output) it was inferred that a negative current (to give a high output) would also be immune to the state changes.

For the October 2018 SET testing the ISL71610M parts were tested four at a time (all within the beam diameter). Each output was buffered and monitored by an oscilloscope that stored a trace whenever triggered. The triggers were set according to the nominal output. When the nominal output was a logic low (GND), the trigger was set for any transition through 0.8V. When the nominal output was logic high (V_{DD}) the trigger was set for any transition through 2.0V. The supply voltage, V_{DD} , was set to either 3.00V or 4.25V. These represent the lowest voltages anticipated for supplies of a 3.3V nominal and for a 5.0V nominal (including use with the ISL70040SEH low side GaN FET driver). The coil current covered the cases of ± 8 mA and 0mA to test for the state change events. The ISL71610M SET count summary appears in [Table 4](#).

Table 4. ISL71610M SET Count Summary

LET, Species (MeV \cdot cm ² /mg)	I_{IN} (mA)	Trigger (V)	V_{DD} (V)	Spike SET counts in 1×10^7 ions/cm ²				Totals
				DUT5	DUT6	DUT7	DUT8	
43 Silver	0	2.0	3.00	13	10	15	19	57
			4.25	8	1	7	17	33
	-8	2.0	3.00	0	1	0	3	4
			3.00	6	8	7	15	36
	+8	0.8	3.00	6	11	5	12	34
			4.25	10	5	11	7	33
20 Copper	0	2.0	3.00	11	6	7	4	28
			4.25	3	5	2	5	15
	-8	2.0	3.00	0	0	0	0	0
			3.00	3	4	4	4	15
	+8	0.8	3.00	6	3	12	5	26
			4.25	5	5	6	2	18

Table 4. ISL71610M SET Count Summary (Continued)

LET, Species (MeV•cm ² /mg)	I _{IN} (mA)	Trigger (V)	V _{DD} (V)	Spike SET counts in 1x10 ⁷ ions/cm ²				Totals
				DUT5	DUT6	DUT7	DUT8	
8.5 Argon	0	2.0	3.00	3	4	4	2	13
			4.25	0	0	0	0	0
	-8		3.00	0	0	0	0	0
			4.25	0	0	0	0	0
	+8	0.8	3.00	1	1	4	2	8
			4.25	0	0	0	0	0

The four ISL71610M units tested October 2018 did not exhibit the state change events. With no assignable cause available it must be assumed that it was only chance that no units exhibited the state change SET seen previously. In addition, it was impossible to test if negative coil current would stop the state change SET. Neither was it possible to determine if the state change SET was stopped at a V_{DD} of 4.25V. Previous testing proved that it was not an issue at V_{DD} of 5.5V. The net ratio of parts exhibiting the state change events is reduced by these results to four out of twelve units.

The captured SET traces for the case of 43MeV•cm²/mg were post processed with a MATLAB® routine to find the duration of the triggering SET. These results were plotted in a form similar to a probability plot and are presented in Figure 35. The longest SET observed was under 39ns, for the case of a high output with a zero current into the coil. For a given V_{DD} the case of a -8mA coil current yielded shorter SET durations as compared to the case with zero current, even though both resulted in nominally high outputs. Durations were the output SET time below 2.0V for a high output, and the duration above 0.8V for a low output.

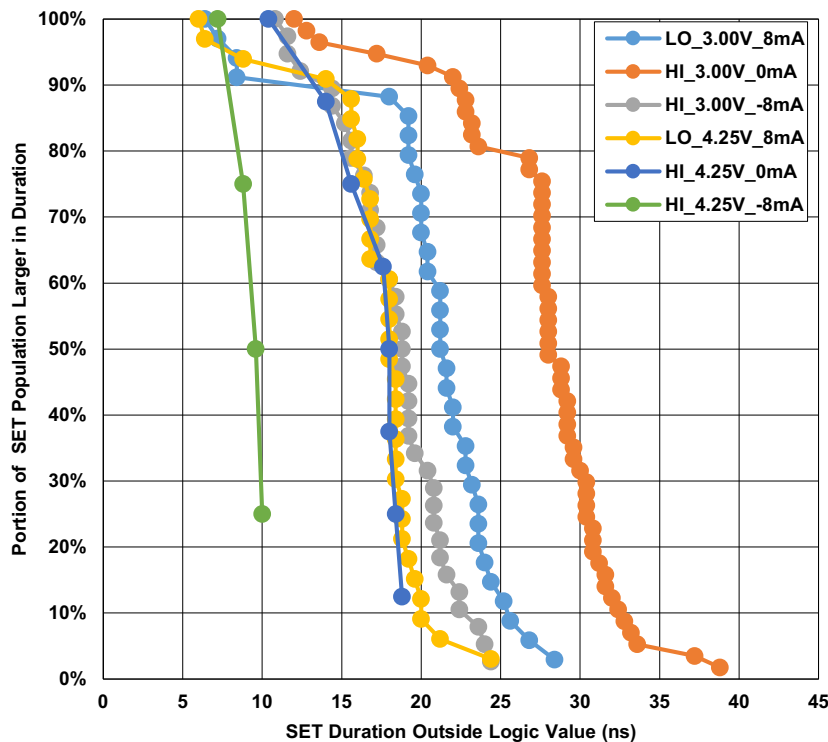


Figure 35. Plot of Cumulative SET Population Portion that is Greater than an Indicated SET Duration

The longest SET transient captured for the ISL71610M at $43\text{MeV}\cdot\text{cm}^2/\text{mg}$ is presented in [Figure 36](#). The twenty foot coaxial cable used to connect the oscilloscope to the buffer on the DUT induced considerable ringing that appears in [Figure 36](#). No filtering was applied at the receiving end so as not to spread the initial events. The initial event in the figure is the sharp spike down that persists below 2.0V for 38.8ns . The smallest duration events barely reached the 2.0V or 0.8 trigger levels and persisted for as little as 6ns .

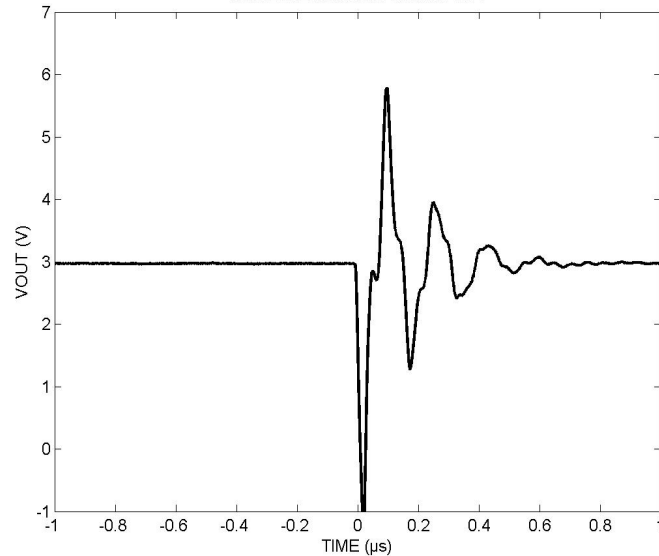


Figure 36. The SET of Extracted Duration of 38.8ns below 2.0V in the First Impulse

5.2.7 Summary

The ISL71610M common barrier isolation was immune to SEDR with normal incidence A_g for an LET of $43\text{MeV}\cdot\text{cm}^2/\text{mg}$ to a fluence of 1×10^7 ion/ cm^2 at an isolation voltage of 500V .

The ISL71610M circuitry was immune to SEL and SEB with normal incidence A_g for an LET of $43\text{MeV}\cdot\text{cm}^2/\text{mg}$ to a fluence of 1×10^7 ion/ cm^2 at a supply voltage of 7.0V .

The ISL71610M had static SET cross sections of at or below $1.8 \times 10^{-6}\text{cm}^2$ when exposed to normal incidence A_g with an LET of $43\text{MeV}\cdot\text{cm}^2/\text{mg}$.

The SET results indicate that the preferred operating conditions are: energize the coil to reduce the incidence of an output state change. The higher V_{DD} supply appears to correlate with lower numbers of transients and no output state changes. The SET results also point to a system design consideration in that the system must be able to survive 40ns wide transients that violate the high and low input threshold voltages of the device they are attached to.

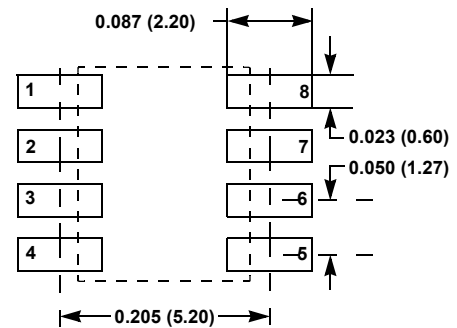
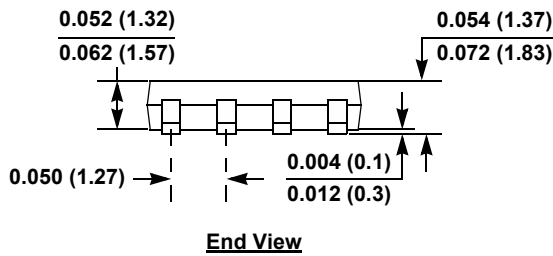
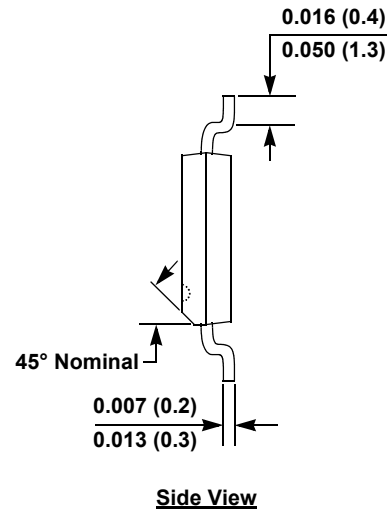
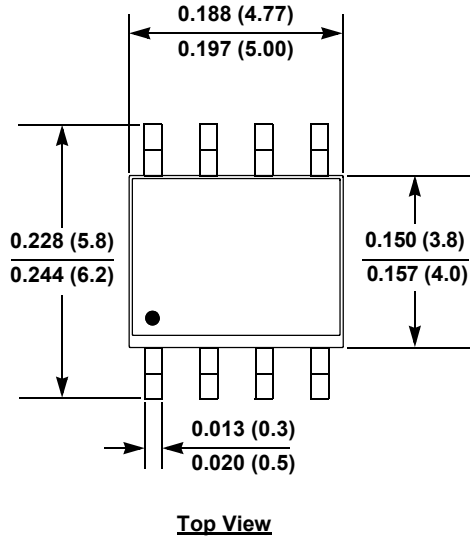
6. Revision History

Rev.	Date	Description
0.00	Nov 8, 2018	Initial Release

7. Package Outline Drawing

For the most recent package outline drawing, see [M8.15G](#).

M8.15G
 8 Lead Narrow Body Small Outline Plastic Package
 Rev 2, 10/18



- Notes:
1. Dimensions in inches (mm); scale = approximately 5X.
 2. Pin spacing is a BASIC dimension; tolerances do not accumulate.

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