High Performance Dual DVGA

Check for Samples: LMH6521

FEATURES

- **OIP3 of 48.5 dBm at 200 MHz**
- **Maximum Voltage Gain of 26 dB**
- **Gain Range of 31.5 dB with 0.5dB Step Size**
- **Channel Gain Matching of ±0.04 dB**
- **Noise Figure of 7.3 dB at Maximum Gain**
- **-3 dB Bandwidth of 1200 MHz**
- **Low Power Dissipation**
- **Independent Channel Power Down**
- **Three Gain Control Modes:**
  - **Parallel Interface**
  - **Serial Interface (SPI)**
  - **Pulse Mode Interface**
- **Temperature Range –40°C to +85°C**
- **Thermally Enhanced, 32–Pin WQFN Package**

APPLICATIONS

- **Cellular Base Stations**
- **Wideband and Narrowband IF Sampling Receivers**
- **Wideband Direct Conversion**
- **Digital Pre-Distortion**
- **ADC Driver**

DESCRIPTION

The LMH6521 contains two high performance, digitally controlled variable gain amplifiers (DVGA).

Both channels of the LMH6521 have an independent, digitally controlled attenuator followed by a high linearity, differential output amplifier. Each block has been optimized for low distortion and maximum system design flexibility. Each channel has a high speed power down mode.

The internal digitally controlled attenuator provides precise 0.5dB gain steps over a 31.5dB range. Serial and parallel programming options are provided. Serial mode programming utilizes the SPI interface. A Pulse mode is also offered where simple up or down commands can change the gain one step at a time.

The output amplifier has a differential output allowing $10V_{PPD}$ signal swings on a single 5V supply. The low impedance output provides maximum flexibility when driving filters or analog to digital converters.

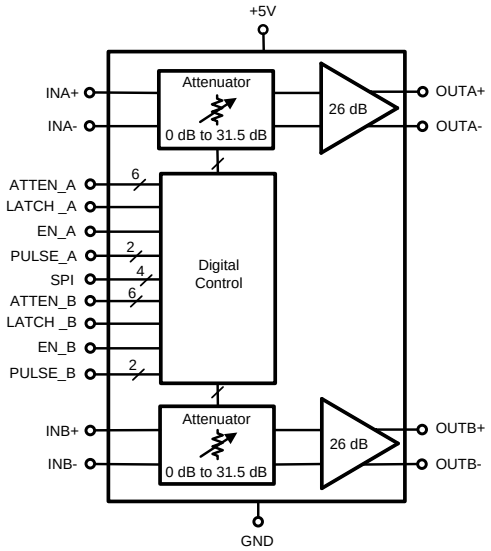

Figure 1. LMH6521 Block Diagram

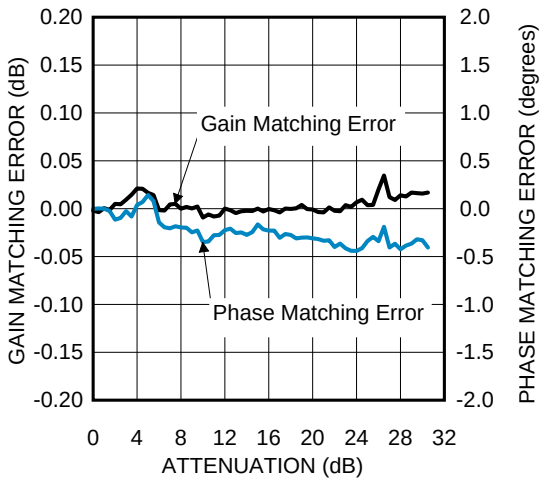

Figure 2. Channel Matching Error (Ch A – Ch B)

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Body Model	2 kV
Machine Model	200V
Charged Device Model	750V
Positive Supply Voltage (Pin 14, 27)	−0.6V to 5.5V
Differential Voltage between Any Two Grounds	<200 mV
Analog Input Voltage Range	−0.6V to V+
Digital Input Voltage Range	−0.6V to 5.5V
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Infrared or Convection (30 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Operating Ratings (1)

Supply Voltage (Pin 14 & 27)	4.75V to 5.25V
Differential Voltage Between Any Two Grounds	<10 mV
Analog Input Voltage Range, AC Coupled	0V to V+
Ambient Temperature Range (2)	−40°C to +85°C
Package Thermal Resistance (θ_{JA})	45°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

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5V Electrical Characteristics (1)

The following specifications apply for single supply with V+ = 5V, Differential V_{OUT} = $4V_{PP}$, R_L= 200Ω, T_A=25°C, f_{in} = 200 MHz, and Maximum Gain (0 attenuation). Boldface limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
Dynamic Performance						
SSBW	3 dB Small Signal Bandwidth			1200		MHz
	Output Noise Voltage	At amplifier output with R_{SOURCE}=200Ω		33		nV/√Hz
	Noise Figure	Source = 200Ω		7.3		dB
OIP3	Output 3rd-Order Intercept Point	f=100MHz, P_O= +4dBm per tone		56		dBm
		f=200MHz, P_O= +4dBm per tone		48.5		
		f=250MHz, P_O= +4dBm per tone		46.5		
OIP2	Output 2nd-Order Intercept Point	f=100MHz, P_O= +4dBm per tone		92		dBm
		f=200MHz, P_O= +4dBm per tone		80		
		f=250MHz, P_O= +4dBm per tone		73		
HD2	2nd Harmonic Distortion	f=200MHz, P_O= +6dBm		–84		dBc
HD3	3rd Harmonic Distortion	f=200MHz, P_O= +6dBm		–83		dBc
P1dB	1dB Compression Point			17		dBm
Analog I/O						
	Input Resistance	Differential		200		Ω
	Input Common Mode Voltage	Self Biased (AC coupled)		2.5		V
	Input Common Mode Voltage Range	Externally Driven (DC coupled)		2–3		V
	Maximum Input Voltage Swing	Differential		11		V_{PPD}
	Output Resistance	Differential		20		Ω
	Maximum Differential Output Voltage Swing	Differential		10		V_{PPD}
CMRR	Common Mode Rejection Ratio	At DC, V_{ID} = 0V, V_{CM} = 2.5 ± 0.5V		80		dB
PSRR	Power Supply Rejection Ratio	At DC, V+ = 5 ± 0.5V, V_{IN} = 2.5V		77		dB
	Channel to Channel Isolation	f = 200 MHz, min. attenuation setting		73		dB
Gain Parameters						
	Maximum Voltage Gain	Gain Code 000000 (min. attenuation), Av = V_O / V_{IN}		26		dB
	Minimum Voltage Gain	Gain Code 111111 (max. attenuation), Av = V_O / V_{IN}		–5.5		dB
	Gain Accuracy			1		%
	Gain Step Size			0.5		dB
	Channel Gain Matching	ChA - ChB, any gain setting		±0.04		dB
	Channel Phase Matching			±0.45		degrees
	Cumulative Gain Error	0 to 12 dB attenuation setting		±0.1		dB
		0 to 24 dB attenuation setting		±0.3		dB
		0 to 31 dB attenuation setting		±0.5		dB
	Cumulative Phase Shift	0 to 12 dB attenuation setting		±0.6		degrees
		0 to 24 dB attenuation setting		±5.3		degrees
		0 to 31 dB attenuation setting		±16.5		degrees
	Gain Step Switching Time			15		ns
	Gain Temperature Sensitivity	0 attenuation setting		2.7		mdB/°C

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. No ensurance of parametric performance is indicated in the electrical tables under conditions different than those tested

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

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5V Electrical Characteristics [1] (continued)

The following specifications apply for single supply with V+ = 5V, Differential V_{OUT} = $4V_{PP}$, R_L= 200Ω, T_A=25°C, f_{in} = 200 MHz, and Maximum Gain (0 attenuation). Boldface limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min [2]	Typ [3]	Max [2]	Units
Power Requirements						
VCC	Supply Voltage		4.75	5.0	5.25	V
ICC	Supply Current	Both Channels Enabled		225	**245**	mA
ICC	Disabled Supply Current	Both Channels		35		mA
All Digital Inputs						
	Logic Compatibility	TTL, 2.5V CMOS, 3.3V CMOS				
VIL	Logic Input Low Voltage			0.5		V
VIH	Logic Input High Voltage			1.8		V
IIH	Logic Input High Input Current	Digital Input Voltage = 5V		200		µA
IIL	Logic Input Low Input Current	Digital Input Voltage = 0V		–60		µA
Parallel and Pulse Mode Timing						
t_{GS}	Setup Time			3		ns
t_{GH}	Hold Time			3		ns
t_{LP}	Latch Low Pulse Width			7		ns
t_{PG}	Pulse Gap between Pulses			20		ns
t_{PW}	Minimum Pulse Width	Pulse Mode		15		ns
t_{RW}	Reset Width			10		ns
Serial Mode Timing and AC Characteristics						
SPI Compatible						
f_{SCLK}	Max Serial Clock Frequency			50		MHz
t_{PH}	SCLK High State Duty Cycle	% of SCLK Period		50		%
t_{PL}	SCLK Low State Duty Cycle	% of SCLK Period		50		%
t_{SU}	Serial Data In Setup Time			2		ns
t_H	Serial Data In Hold Time			2		ns
t_{OZD}	Serial Data Out TRI-STATE-to-Driven Time	Referenced to Negative edge of SCLK		10		ns
t_{OD}	Serial Data Out Output Delay Time	Referenced to Negative edge of SCLK		10		ns
t_{CSS}	Serial Chip Select Setup Time	Referenced to Positive edge of SCLK		5		ns

CONNECTION DIAGRAM

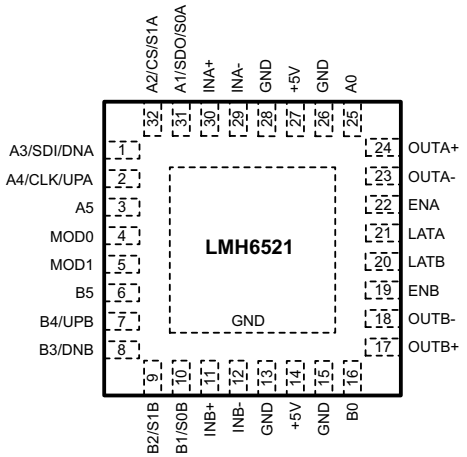

Figure 3. 32-Pin WQFN Package-Top View

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PIN DESCRIPTIONS

Pin Number	Symbol	Description
Analog I/O		
30, 11	INA+, INB+	Amplifier non—inverting input. Internally biased to mid supply. Input voltage should not exceed V+ or go below GND by more than 0.5V.
29, 12	INA−, INB−	Amplifier inverting input. Internally biased to mid supply. Input voltage should not exceed V+ or go below GND by more than 0.5V.
24, 17	OUTA+, OUTB+	Amplifier non—inverting output. Externally biased to 0V.
23, 18	OUTA−, OUTB−	Amplifier inverting output. Externally biased to 0V.
Power		
13, 15, 26, 28, center pad	GND	Ground pins. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is internally bonded to the ground pins.
14, 27	+5V	Power supply pins. Valid power supply range is 4.75V to 5.25V.
Common Control Pins		
4, 5	MOD0, MOD1	Digital Mode control pins. These pins float to the logic hi state if left unconnected. See Application Information for Mode settings.
22, 19	ENA, ENB	Enable pins. Logic 1 = enabled state. See Application Information for operation in serial mode.
Digital Inputs Parallel Mode (MOD1 = 1, MOD0 = 1)		
25, 16	A0, B0	Attenuation bit zero = 0.5dB step. Gain steps down from maximum gain (000000 = Maximum Gain).
31, 10	A1, B1	Attenuation bit one = 1dB step.
32, 9	A2, B2	Attenuation bit two = 2dB step.
1, 8	A3, B3	Attenuation bit three = 4dB step.
2, 7	A4, B4	Attenuation bit four = 8dB step.
3, 6	A5, B5	Attenuation bit five = 16dB step.
21, 20	LATA, LATB	Latch pins. Logic zero = active, logic 1 = latched. Gain will not change once latch is high. Connect to ground if the latch function is not desired.
Digital Inputs Serial Mode (MOD1 =1, MOD0 = 0) SPI compatible		
2	CLK	Serial Clock
1	SDI	Serial Data In. See Application Information for more details.
32	CSb	Serial Chip Select (Active Low).
31	SDO	Serial Data Out.
3, 4, 6, 7, 8, 9, 10, 16, 20, 21, 25	GND	Pins unused in Serial Mode, connect to DC ground.
Digital Inputs Pulse Mode (MOD1 = 0, MOD0 = 1)		
2, 7	UPA, UPB	Up pulse pin. A logic 0 pulse will increase gain one step.
1, 8	DNA, DNB	Down pulse pin. A logic 0 pulse will decrease gain one step.
1 & 2 or 7 & 8		Pulsing both pins together will reset the gain to maximum gain.
31, 32	S0A, S1A	Step size zero and step size 1. (0,0) = 0.5dB; (0, 1)= 1dB; (1,0) = 2dB, and (1, 1)= 6dB.
10, 9	S0B, S1B	Step size zero and step size 1. (0,0) = 0.5dB; (0, 1)= 1dB; (1,0) = 2dB, and (1, 1)= 6dB.
3, 5, 6, 16, 25	GND	Pins unused in Pulse Mode, connect to DC ground.

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DIGITAL CONTROL MODE PIN FUNCTIONS

Pin Number	Parallel Mode	Serial Mode	Pulse Mode
1	A3	SDI	DNA
2	A4	CLK	UPA
3	A5	NC	GND
4 (MOD0)	LOGIC HIGH (MOD0=1)	LOGIC LOW (MOD0=0)	LOGIC HIGH (MOD0=1)
5 (MOD1)	LOGIC HIGH (MOD1=1)	LOGIC HIGH (MOD1=1)	LOGIC LOW (MOD1=0)
6	B5	GND	GND
7	B4	NC	UPB
8	B3	NC	DNB
9	B2	NC	S1B
10	B1	NC	S0B
11	INB+		
12	INB-		
13	GND		
14	+5V		
15		GND	
16	B0	GND	GND
17	OUTB+		
18	OUTB-		
19	ENB		
20	LATB	GND	GND
21	LATA	GND	GND
22	ENA		
23	OUTA-		
24	OUTA+		
25	A0	NC	GND
26	GND		
27	+5V		
28	GND		
29	INA-		
30	INA+		
31	A1	SDO	S0A
32	A2	CS	S1A

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Typical Performance Characteristics

V+ = 5V, Differential V_{OUT} = $4V_{PP}$, R_L = 200Ω, T_A=25 °C, f_{in} = 200 MHz, and Maximum Gain (0 Attenuation)

Frequency Response 2dB Gain Steps

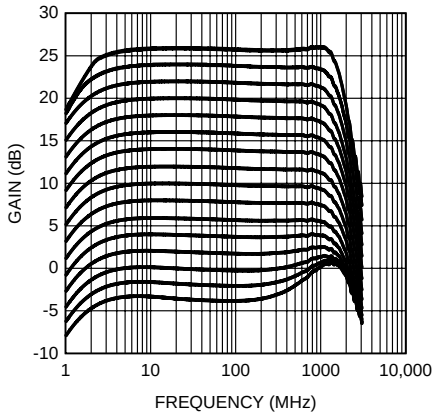

Figure 4.

Gain Flatness vs. Temperature

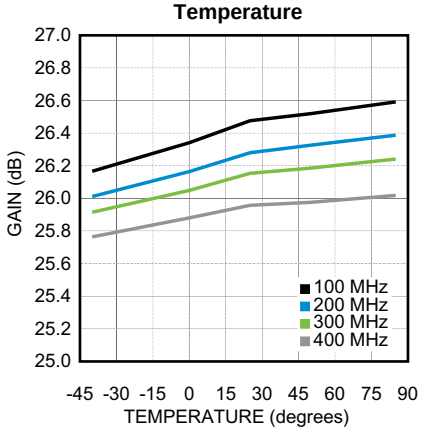

Figure 5.

OIP3 vs. Frequency

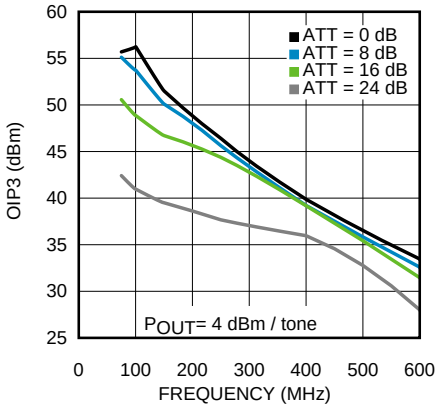

Figure 6.

OIP3 vs. Temperature

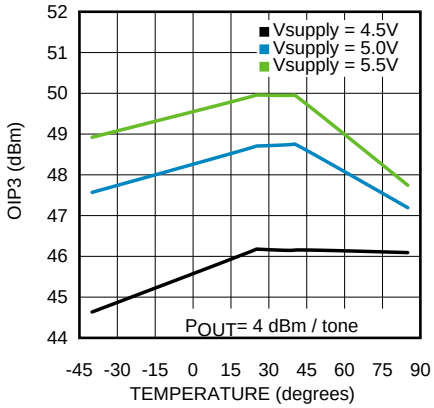

Figure 7.

OIP3 vs. Pout

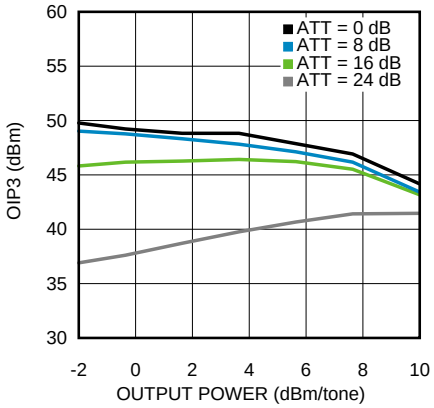

Figure 8.

Third Order Intermodulation Products vs. Frequency

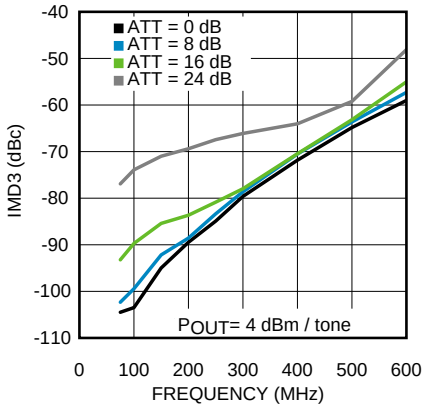

Figure 9.

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Typical Performance Characteristics (continued)

V+ = 5V, Differential V_{OUT} = 4V_{PP}, R_L = 200Ω, T_A=25 °C, f_{in} = 200 MHz, and Maximum Gain (0 Attenuation)

Third Order Harmonic Distortion vs. Frequency

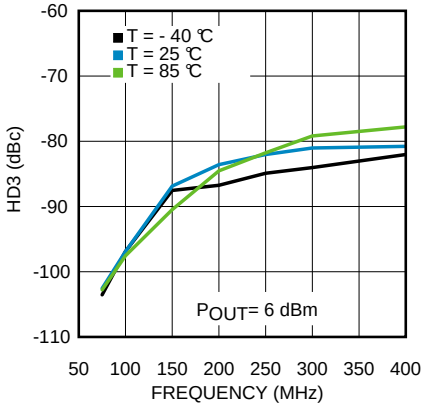

Figure 10.

Second Order Harmonic Distortion vs. Attenuation

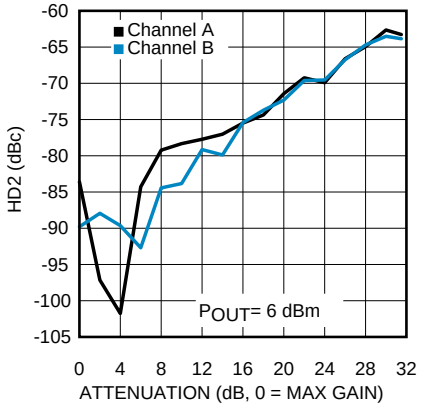

Figure 11.

Third Order Harmonic Distortion vs. Attenuation

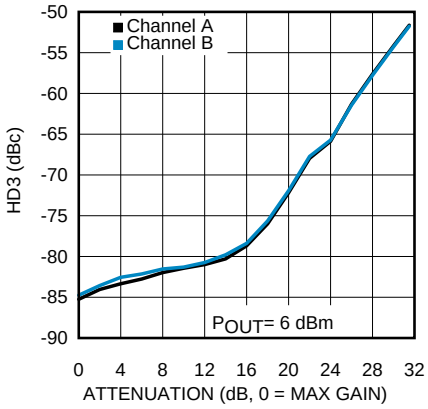

Figure 12.

Second Order Harmonic Distortion vs. Frequency

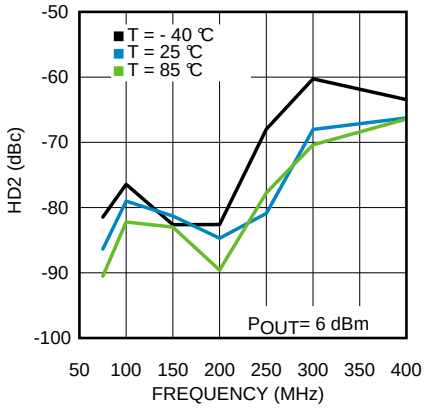

Figure 13.

Second Order Harmonic Distortion at 100 MHz

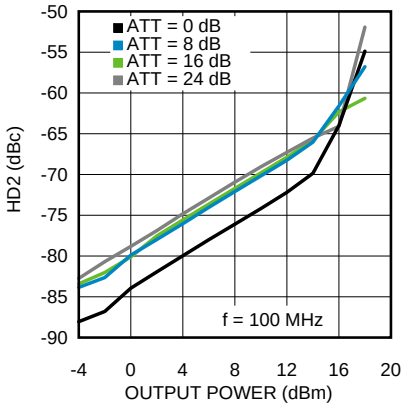

Figure 14.

Third Order Harmonic Distortion at 100 MHz

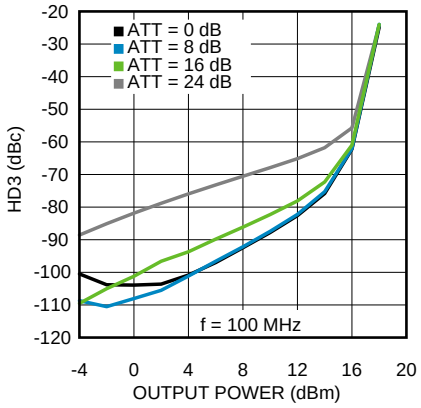

Figure 15.

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Typical Performance Characteristics (continued)

V+ = 5V, Differential V_{OUT} = 4V_{PP}, R_L = 200Ω, T_A=25 °C, f_{in} = 200 MHz, and Maximum Gain (0 Attenuation)

Second Order Harmonic Distortion at 200 MHz

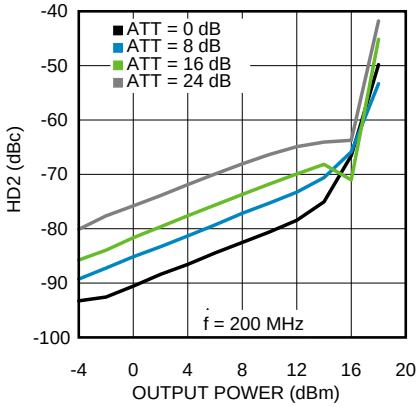

Figure 16.

Third Order Harmonic Distortion at 200 MHz

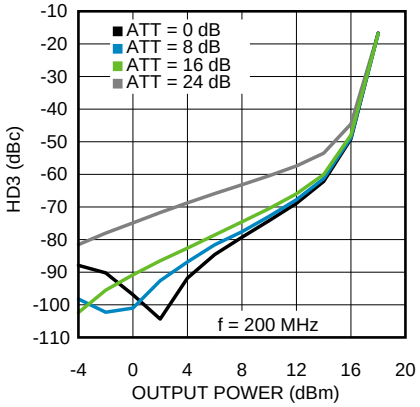

Figure 17.

Cumulative Gain Error

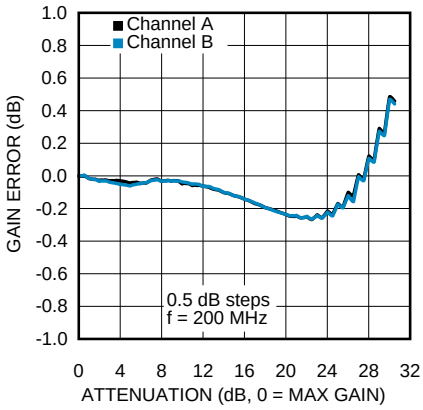

Figure 18.

Cumulative Phase Shift

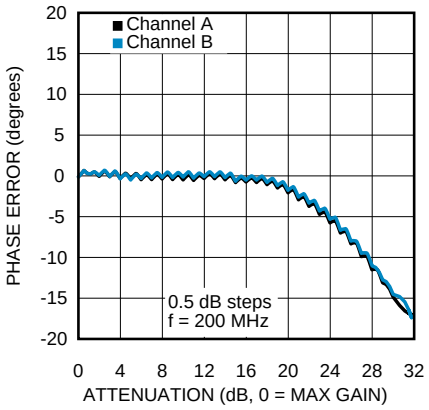

Figure 19.

Noise Figure vs. Frequency

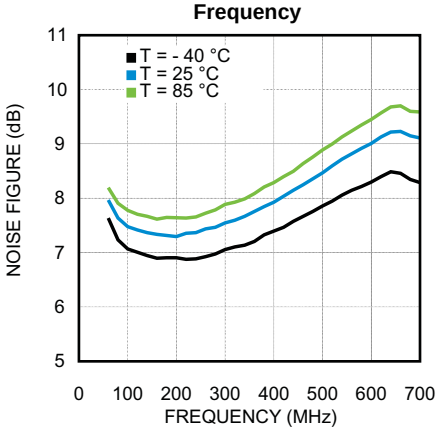

Figure 20.

Noise Figure vs. Attenuation

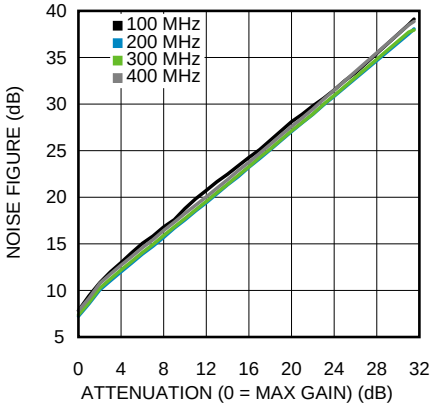

Figure 21.

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Typical Performance Characteristics (continued)

V+ = 5V, Differential V_{OUT} = 4V_{PP}, R_L = 200Ω, T_A=25 °C, f_{in} = 200 MHz, and Maximum Gain (0 Attenuation)

Supply Current vs. Temperature

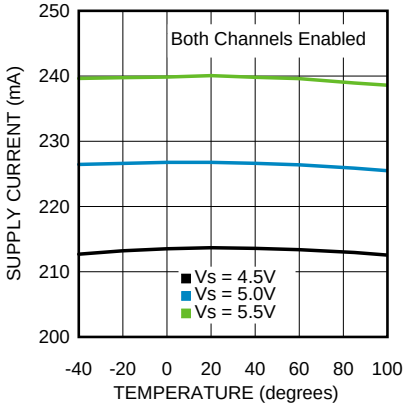

Figure 22.

Channel To Channel Isolation

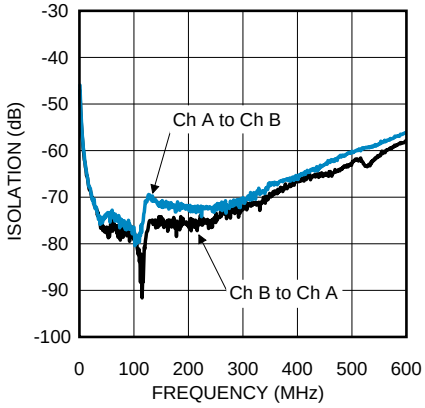

Figure 23.

Input Impedance

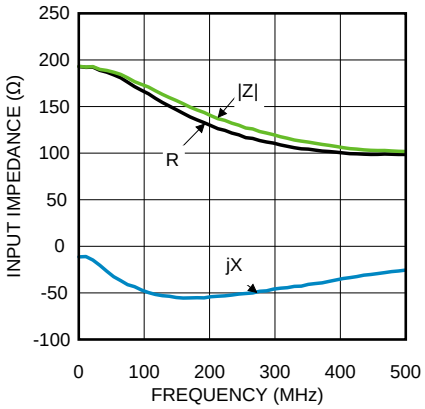

Figure 24.

Output Impedance

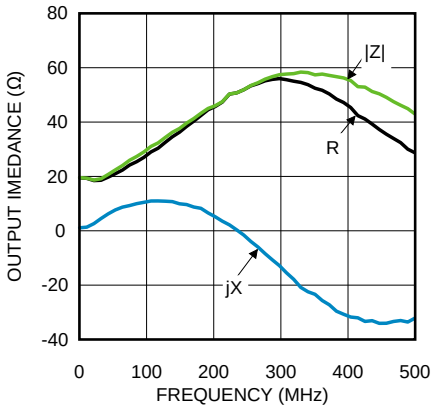

Figure 25.

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APPLICATION INFORMATION

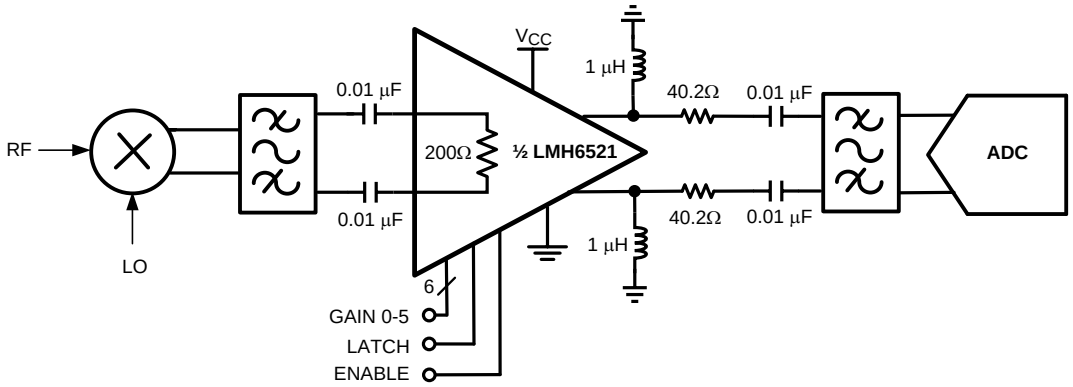

Figure 26. LMH6521 Typical Application

INTRODUCTION

The LMH6521 is a dual, digitally controlled variable gain amplifier designed for narrowband and wideband intermediate frequency sampling applications. The LMH6521 is optimized for accurate 0.5 dB gain steps with exceptional gain and phase matching between channels combined with low distortion products. Gain matching error is less than ±0.05 dB and phase matching error less than ±0.5 degrees over the entire attenuation range. This makes the LMH6521 ideal for driving analog-to-digital converters where high linearity is necessary. Figure 26 shows a typical application circuit.

The LMH6521 has been designed for AC coupled applications and has been optimized to operate at frequencies greater than 3 MHz.

BASIC CONNECTIONS

A voltage between 4.75 V and 5.25 V should be applied to the supply pin labeled +5V. Each supply pin should be decoupled with a additional capacitance along with some low inductance, surface-mount ceramic capacitor of 0.01uF as close to the device as possible where space allows.

The outputs of the LMH6521 are low impedance devices that need to be connected to ground with 1uH RF chokes and require ac-coupling capacitors of 0.01uF. The input pins are self biased to 2.5V and should be ac-coupled with 0.01uF capacitors as well. The output RF inductors and ac-coupling capacitors are the main limitations for operating at low frequencies.

Each channel of the LMH6521 consists of a digital step attenuator followed by a low distortion 26 dB fixed gain amplifier and a low impedance output stage. The gain is digitally controlled over a 31.5 dB range from +26dB to −5.5dB. The LMH6521 has a 200Ω differential input impedance and a low 20Ω differential output impedance.

To enable each channel of the LMH6521, the ENA and ENB pins can be left to float, which internally is connected high with a weak pull-up resistor. Externally connecting ENA and ENB to ground will disable the channels of the LMH6521 and reduce the current consumption to 17.5mA per channel.

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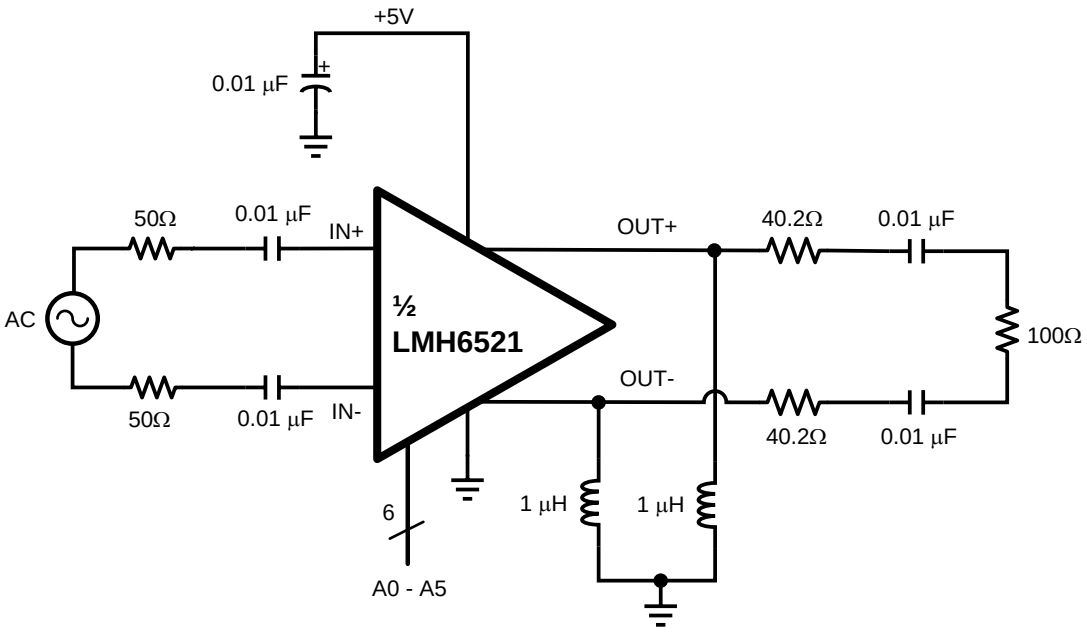

Figure 27. Basic Operating Connection

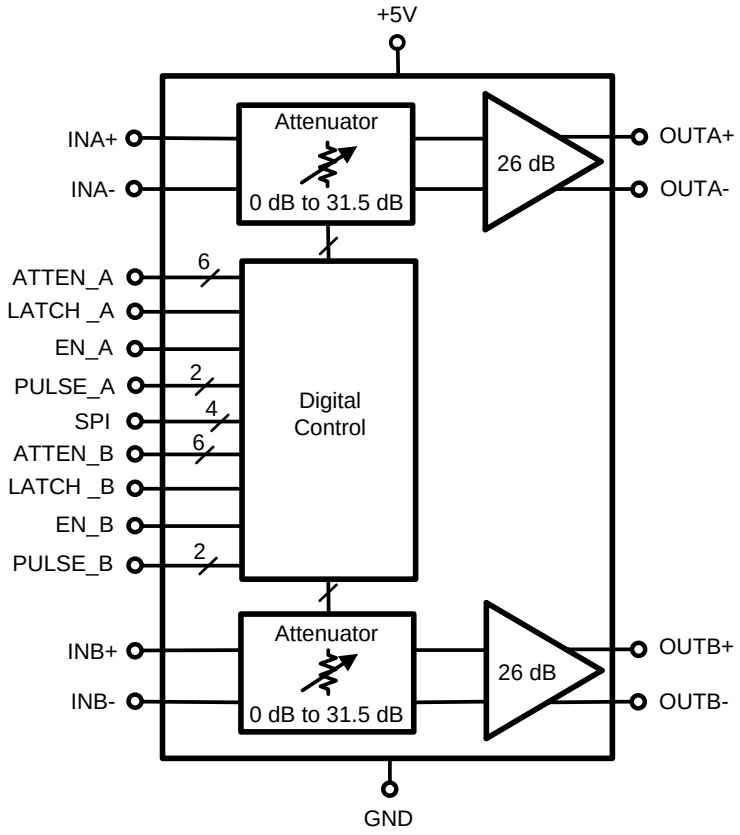

Figure 28. LMH6521 Block Diagram

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INPUT CHARACTERISTICS

The LMH6521 input impedance is set by internal resistors to a nominal 200Ω. At higher frequencies device parasitic reactances will start to impact the input impedances. Refer to Figure 24 in Typical Performance Characteristics for more details

For many AC coupled applications the impedance can be easily changed using LC circuits to transform the actual impedance to the desired impedance.

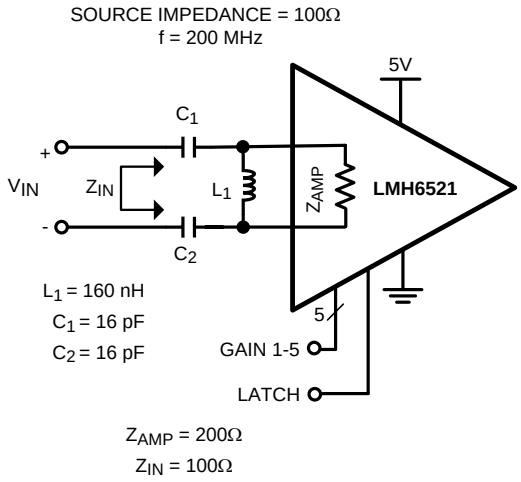

Figure 29. Differential 200Ω LC Conversion Circuit

In Figure 29 a circuit is shown that matches the amplifier 200Ω input with a source impedance of 100Ω.

To avoid undesirable signal transients the LMH6521 should not be powered on with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs.

OUTPUT CHARACTERISTICS

The LMH6521 has a low output impedance very similar to a traditional operational amplifier output. This means that a wide range of load impedance can be driven with minimal gain loss. Matching load impedance for proper termination of filters is as easy as inserting the proper value of resistor between the filter and the amplifier. This flexibility makes system design and gain calculations very easy. The LMH6521 was designed to run from a single 5V supply. In spite of this low supply voltage the LMH6521 is still able to deliver very high power gains when driving low impedance loads.

OUTPUT CONNECTIONS

The LMH6521, like most high frequency amplifiers, is sensitive to loading conditions on the output. Load conditions that include small amounts of capacitance connected directly to the output can cause stability problems. An example of this is shown in Figure 30. A more sophisticated filter may require better impedance matching. Refer to Figure 41 for an example filter configuration and table Table 5 for some IF filter components values.

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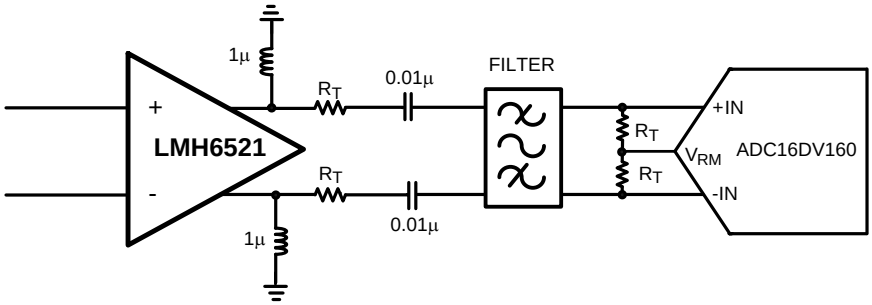

Figure 30. Example Output Configuration

The outputs of the LMH6521 need to be biased to near ground potential. On the evaluation board, 1µH inductors are installed to provide proper output biasing. The bias current is approximately 36mA per output pin and is not a function of the load condition, which makes the LMH6521 robust to handle various output load conditions while maintaining superior linearity as shown in Figure 31. With large inductors and high operating frequencies the inductor will present a very high impedance and will have minimal AC current. If the inductor is chosen to have a smaller value, or if the operating frequency is very low there could be enough AC current flowing in the inductor to become significant. Make sure to check the inductor datasheet to not exceed the maximum current limit.

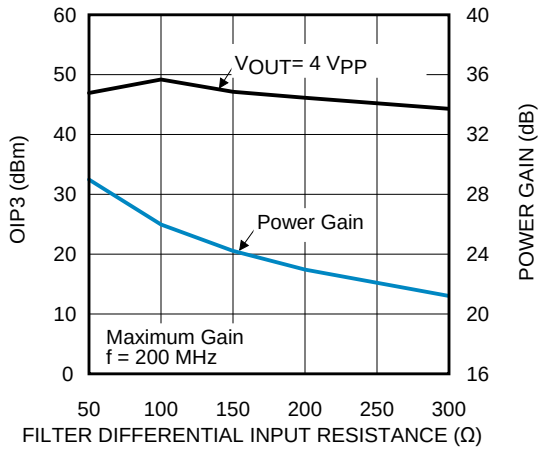

Figure 31. OIP3 vs Amplifier Load Resistance

DIGITAL CONTROL

The LMH6521 will support three modes of gain control, parallel mode, serial mode (SPI compatible) and pulse mode. Parallel mode is fastest and requires the most board space for logic line routing. Serial mode is compatible with existing SPI compatible systems. The pulse mode is both fast and compact, but must step through intermediate gain steps when making large gain changes.

Pins MOD0 and MOD1 are used to configure the LMH6521 for the three gain control modes. MOD0 and MOD1 have weak pull-up resistors to an internal 2.5V reference but is designed for 2.5V-5V CMOS logic levels. MOD0 and MOD1 can be externally driven (LOGIC HIGH) to voltages between 2.5V to 5V to configure the LMH6521 into one of the three digital control modes. Some pins on the LMH6521 have different functions depending on the digital control mode. These functions are shown in Digital Control Modes Pin Functions.

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PARALLEL MODE (MOD1= 1, MOD0 = 1)

When designing a system that requires very fast gain changes parallel mode is the best selection. Refer to for pin definitions of the LMH6521 in parallel mode.

The LMH6521 has a 6-bit gain control bus as well as latch pins LATA and LATB for channels A and B. When the latch pin is low, data from the gain control pins is immediately sent to the gain circuit (i.e. gain is changed immediately). When the latch pin transitions high the current gain state is held and subsequent changes to the gain set pins are ignored. To minimize gain change glitches multiple gain control pins should not change while the latch pin is low. Gain glitches could result from timing skew between the gain set bits. This is especially the case when a small gain change requires a change in state of three or more gain control pins. If continuous gain control is desired the latch pin can be tied to ground. This state is called transparent mode and the gain pins are always active. In this state the timing of the gain pin logic transitions should be planned carefully to avoid undesirable transients

ENA and ENB pins are provided to reduce power consumption by disabling the highest power portions of the LMH6521. The gain register will preserve the last active gain setting during the disabled state. These pins will float high and can be left disconnected if they won't be used. If the pins are left disconnected a 0.01uF capacitor to ground will help prevent external noise from coupling into these pins.

Figure 32, Figure 33, and Figure 34 show the various connections in parallel mode with respect to the latch pin.

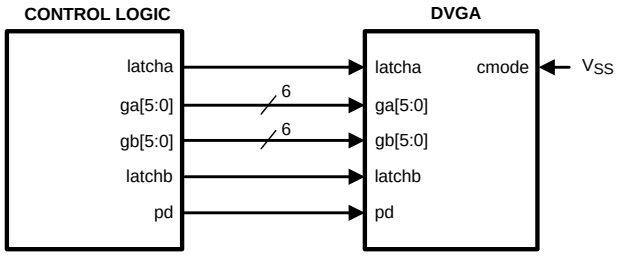

Figure 32. Parallel Mode Connection for Fastest Response

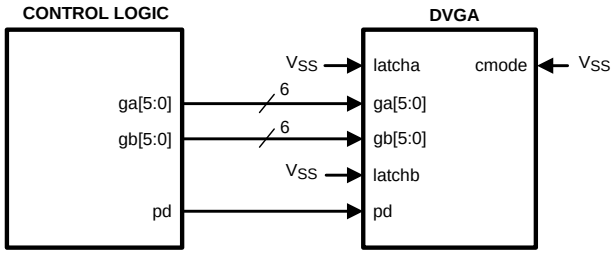

Figure 33. Parallel Mode Connection Not Using Latch Pins (Latch pins tied to logic low state)

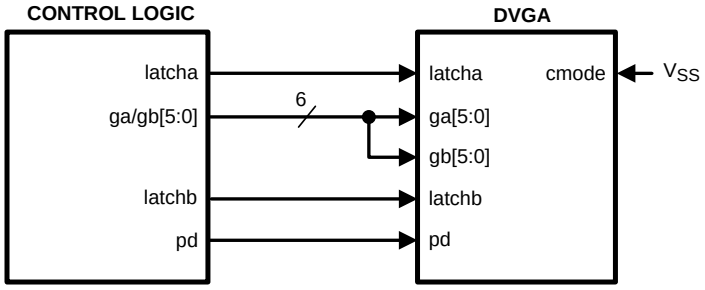

Figure 34. Parallel Mode Connection Using Latch Pins to Mulitplex Digital Data

SERIAL MODE — SPI COMPATIBLE INTERFACE (MOD1= 1, MOD0 = 0)

Serial interface allows a great deal of flexibility in gain programming and reduced board complexity. Using only 4 wires for both channels allows for significant board space savings. The trade off for this reduced board complexity is slower response time in gain state changes. For systems where gain is changed only infrequently or where only slow gain changes are required serial mode is the best choice. Refer to table for pin definitions of the LMH6521 in serial mode.

The serial interface is a generic 4-wire synchronous interface that is compatible with SPI standard interfaces and used on many microcontrollers and DSP controllers.

The serial mode is active when the two mode pins are set as follows: MOD1=1, MOD0=0). In this configuration the pins function as shown in the table. The SPI interface uses the following signals: clock input (CLK), serial data in (SDI), serial data out, and serial chip select (CS)

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ENA and ENB pins are active in serial mode. For fast disable capability these pins can be used and the serial register will hold the last active gain state. These pins will float high and can be left disconnected for serial mode. The serial control bus can also disable the DVGA channels, but at a much slower speed. The serial enable function is an AND function. For a channel to be active both the enable pin and the serial control register must be in the enabled state. To disable a channel either method will suffice. See Typical Performance Characteristics for disable and enable timing information.

LATA and LATB pins are not active during serial mode.

The serial clock pin CLK is used to register the input data that is presented on the SDI pin on the rising edge; and to source the output data on the SDO pin on the falling edge. User may disable clock and hold it in the low state, as long as the clock pulse-width minimum specification is not violated when the clock is enabled or disabled.

The chip select pin CS starts a new register access with each assertion - i.e., the SDATA field protocol is required. The user is required to deassert this signal after the 16th clock. If the SCSb is deasserted before the 16th clock, no address or data write will occur. The rising edge captures the address just shifted-in and, in the case of a write operation, writes the addressed register. There is a minimum pulse-width requirement for the deasserted pulse - which is specified in Electrical Characteristics.

SDI is an input pin for the serial data. It must observe setup/hold requirements with respect to the SCLK. Each cycle is 16-bits long

SDO is the data output pin and is normally at TRI-STATE and is driven only when SCSb is asserted. Upon SCSb assertion, contents of the register addressed during the first byte are shifted out with the second 8 SCLK falling edges. Upon power-up, the default register address is 00h

The SDO internal driver circuit is an open collector device with a weak pull-up resistor to an internal 2.5V reference. It is 5V tolerant so an external pull-up resistor can connect to 2.5V, 3.3V or 5V as shown in Figure 36. However, the external pull-up resistor should be chosen to limit the current to 11mA or less. Otherwise the SDO logic low output level (V_{OL} may not achieve close to ground and in extreme case could cause problem for FPGA input gate. Using minimum values for external pull-up resistor is a good to maximize speed for SDO signal. So if high SPI clock frequency is needed then minimum value external pull-up resistor is the best choice as shown in Figure 36.

Each serial interface access cycle is exactly 16 bits long as shown in Figure 35. Each signal's function is described below. The read timing is shown in Figure 37, while the write timing is shown in figure Figure 38.

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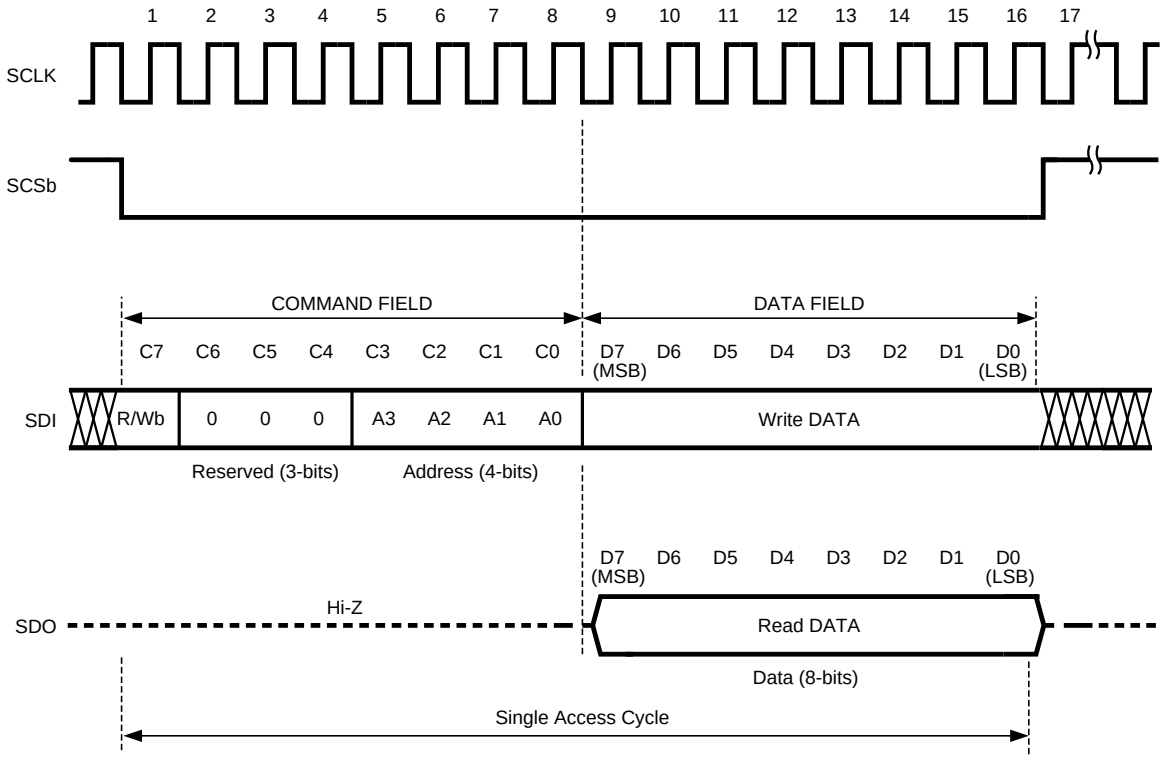

Figure 35. Serial Interface Protocol (SPI compatible)

R/Wb	Read / Write bit. A value of 1 indicates a read operation, while a value of 0 indicates a write operation.
Reserved	Not used. Must be set to 0.
ADDR:	Address of register to be read or written.
DATA	In a write operation the value of this field will be written to the addressed register when the chip select pin is deasserted. In a read operation this field is ignored.

Table 1. Serial Word Format for LMH6521

C7	C6	C5	C4	C3	C2	C1	C0
0= write 1=read	0	0	0	0	0	0	0=Ch A 1=Ch B

Table 2. Serial Word Format for LMH6521 (cont)

Enable	Gb5	Gb4	Gb3	Gb2	Gb1	Gb0	RES
0=Off 1=On	1=+16dB	1=+8dB	1=+4dB	1=+2dB	1=+1dB	1=+0.5dB	0

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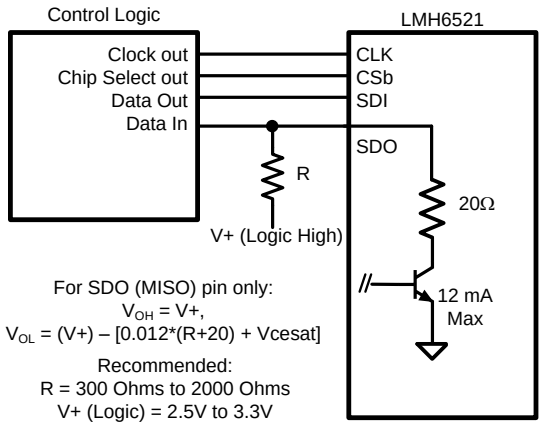

Figure 36. Serial Mode 4–wire Connection

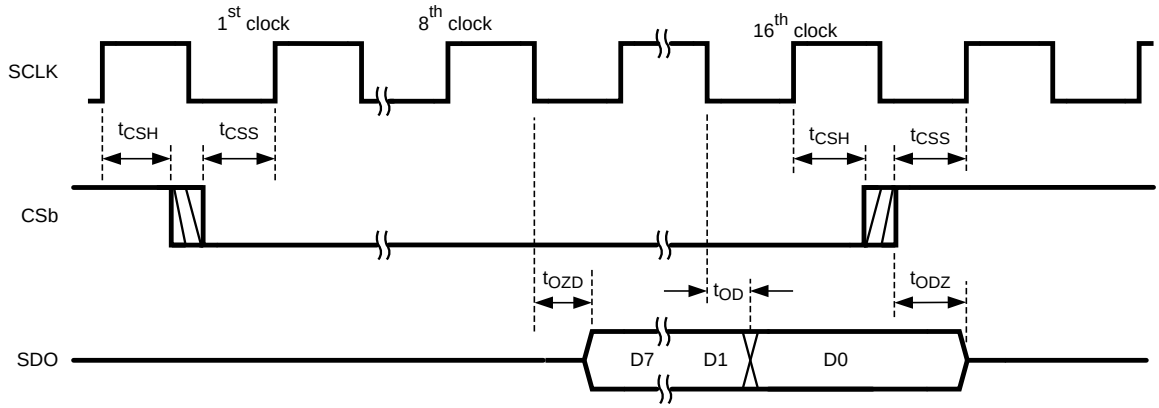

Figure 37. Read Timing

Table 3. Read Timing
Data Output on SDO Pin

Parameter	Description
t_{CSH}	Chip select hold time
t_{CSS}	Chip select setup time
t_{OZD}	Initial output data delay
t_{ODZ}	High impedance delay
t_{OD}	Output data delay

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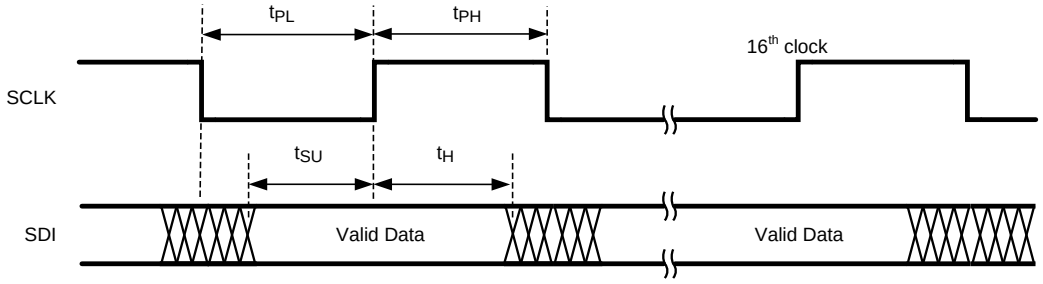


Figure 38. Write Timing, Data Written to SDI Pin

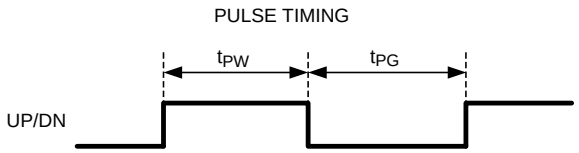
Table 4. Write Timing Data Input on SDI Pin

Parameter	Description
t_{PL}	Minimum clock low time (clock duty dycle)
t_{PH}	Minimum clock high time (clock duty cycle)
t_{SU}	Input data setup time
t_{H}	Input data hold time

PULSE MODE (MOD1= 0, MOD0 = 1)

Pulse mode is a simple yet fast way to adjust gain settings. Using only two control lines per channel the LMH6521 gain can be changed by simple up and down signals. Gain step sizes is selectable either by hard wiring the board or using two additional logic inputs. For a system where gain changes can be stepped sequentially from one gain to the next and where board space is limited this mode may be the best choice. The ENA and ENB pins are fully active during pulse mode, and the channel gain state is preserved during the disabled state. Refer to for pin definitions of the LMH6521 in pulse mode.

In this mode the gain step size can be selected from a choice of 0.5, 1, 2 or 6dB steps. During operation the gain can be quickly adjusted either up or down one step at a time by a negative pulse on the UP or DN pins. As shown in Figure 39 each gain step pulse must have a logic high state of at least t_{PW}= 20 ns and a logic low state of at least t_{PG}= 20 ns for the pulse to register as a gain change signal.



To provide a known gain state there is a reset feature in pulse mode. To reset the gain to maximum gain both the UP and DN pins must be strobed low together as shown in Figure 39. There must be an overlap of at least t_{RW}= 20 ns for the reset to register.

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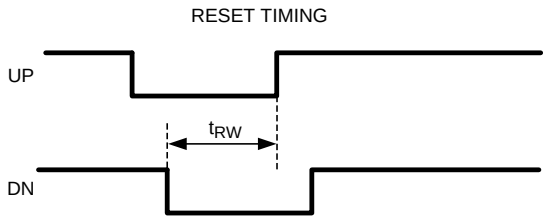

Figure 39. Pulse Mode Timing

THERMAL MANAGEMENT

The LMH6521 is packaged in a thermally enhanced WQFN package and features an exposed pad that is connected to the GND pins. It is recommended that the exposed pad be attached directly to a large power supply ground plane for maximum heat dissipation. The thermal advantage of the WQFN package is fully realized only when the exposed die attach pad is soldered down to a thermal land on the PCB board with the through vias planted underneath the thermal land. The thermal land can be connected to any ground plane within the PCB. However, it is also very important to maintain good high speed layout practices when designing a system board.

The LMH6521EVAL evaluation board implemented an eight metal layer pcb with (a) 4 oz. copper inner ground planes (b) additonal through vias and (c) maximum bottom layer metal coverage to assist with device heat dissipation. These pcb design techniques assisted with the heat dissipation of the LMH6521 to optimize distortion performance. Please refer to the LMH6521EVAL evaluation board application note AN–2045 SNOA551 for suggested layout techniques.

Package information is available on the Texas Instruments web site.

http://www.ti.com/packaging

INTERFACE TO ADC

The LMH6521 was designed to be used with TI's high speed ADC's. As shown in Figure 26, AC coupling provides the best flexibility especially for IF sub-sampling applications.

The inputs of the LMH6521 will self bias to the optimum voltage for normal operation. The internal bias voltage for the inputs is approximately mid rail which is 2.5V with the typical 5V power supply condition. In most applications the LMH6521 input will need to be AC coupled.

The LMH6521 output common mode voltage is biased to 0V and has a maximum differential output voltage swing of $10V_{PPD}$ as shown in Figure 40. This means that for driving most ADCs AC coupling is required. Since most often a band pass filter is desired between the amplifier and ADC the bandpass filter can be configured to block the DC voltage of the amplifier output from the ADC input. Figure 41 shows a wideband bandpass filter configuration that could be designed for a 200Ω impedance system for various IF frequencies.

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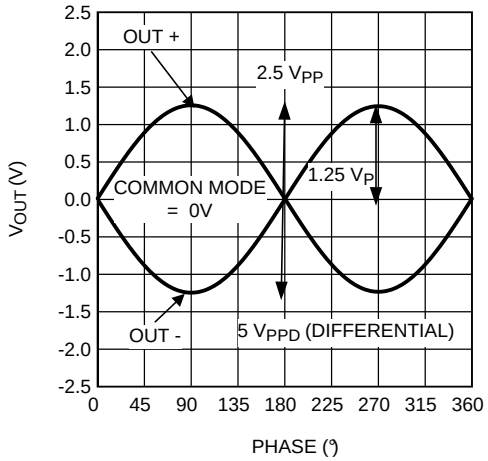

Figure 40. Output Voltage with Respect to Output Common Mode

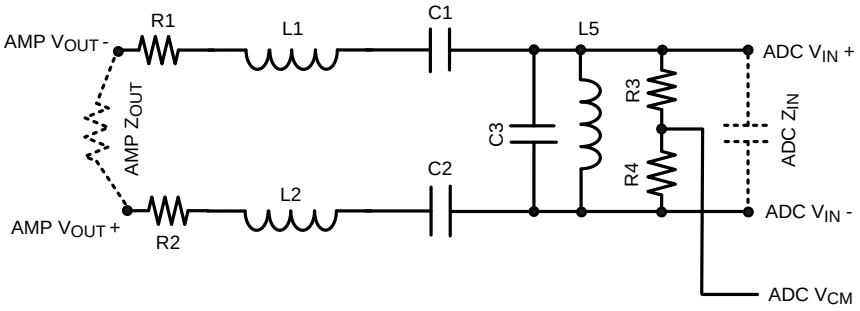

Figure 41. Wideband Bandpass Filter

Table Table 5 show values for some common IF frequencies for Figure 41. The filter shown in Figure 41 offers a good compromise between bandwidth, noise rejection and cost. This filter topology works best with the 12 to 16 bit analog to digital converters shown in the Table 7.

Table 5. IF Frequency Bandpass Filter Component Values

Center Frequency	75 MHz	150 MHz	180 MHz	250 MHz
Bandwidth	40 MHz	60 MHz	75 MHz	100 MHz
R1, R2	90 Ω	90 Ω	90 Ω	90 Ω
L1, L2	390 nH	370 nH	300 nH	225 nH
C1, C2	10 pF	3 pF	2.7 pF	1.9 pF
C3	22 pF	19 pF	15 pF	11 pF
L5	220 nH	62 nH	54 nH	36 nH
R3, R4	100 Ω	100 Ω	100 Ω	100 Ω

An alternate narrowband filter approach is presented in Figure 42. The narrow band-pass antialiasing filter between the LMH6521 and ADC16DV160 attenuates the output noise of the LMH6521 outside the Nyquist zone helping to preserve the available SNR of the ADC. Figure 42 shows a 1:4 input transformer used to match the 200Ω balanced input of the LMH6521 to the 50 unbalanced source to minimize insertion lost at the input. Figure 42 shows the LMH6521 driving the ADC16DV160 (16–bit ADC). The band-pass filter is a 3rd order 100Ω matched tapped-L configured for a center frequency of 192MHz with a 20MHz bandwidth across the differential inputs of the ADC16DV160. The ADC16DV160 is a dual channel 16–bit ADC with maximum sampling rate of 160 MSPS. Using a 2–tone large input signal with the LMH6521 set to maximum gain (26dB) to drive an input signal level at the ADC of –1dBFS, the SNR and SFDR results are shown in table below.

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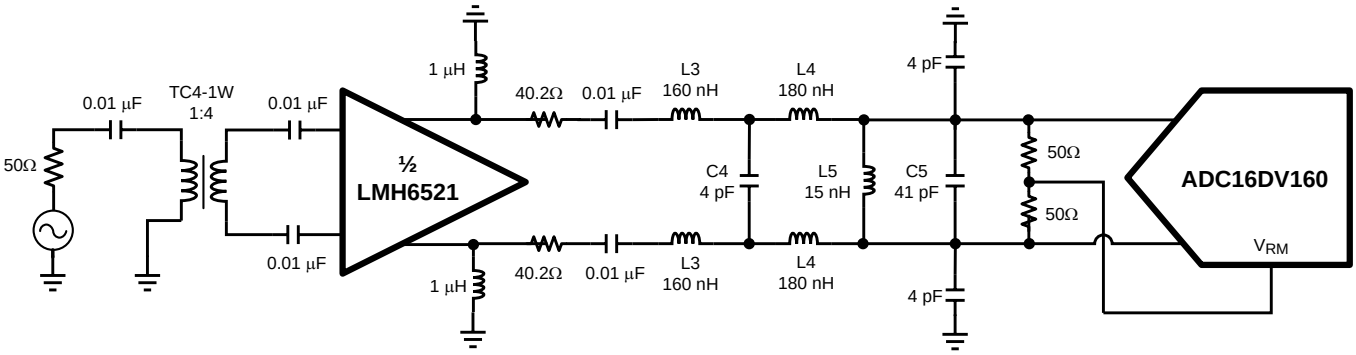
Table 6. LMH6521+BPF+ADC16DV160 vs Typical ADC16DV160 Specifications

Configuraton	ADC Input	SNR (dBFS)	SFDR (dBFS)
LMH6521+BPF+ADC16DV160	–1dBFS	75.5	82
ADC16DV160 only	–1dBFS	76	89

POWER SUPPLIES

The LMH6521 was designed primarily to be operated on 5V power supplies. The voltage range for V_{CC} is 4.75V to 5.25V. When operated on a board with high speed digital signals it is important to provide isolation between digital signal noise and the LMH6521 inputs. The SP16160CH1RB reference board provides an example of good board layout.



Center Frequency is 192MHz with a 20MHz Bandwidth. Designed for 200Ω Impedance.

Figure 42. Narrowband Tapped-L Bandpass Filter

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Table 7. COMPATIBLE HIGH SPEED ANALOG TO DIGITAL CONVERTERS

Product Number	Max Sampling Rate (MSPS)	Resolution	Channels
ADC12L063	62	12	SINGLE
ADC12DL065	65	12	DUAL
ADC12L066	66	12	SINGLE
ADC12DL066	66	12	DUAL
CLC5957	70	12	SINGLE
ADC12L080	80	12	SINGLE
ADC12DL080	80	12	DUAL
ADC12C080	80	12	SINGLE
ADC12C105	105	12	SINGLE
ADC12C170	170	12	SINGLE
ADC12V170	170	12	SINGLE
ADC14C080	80	14	SINGLE
ADC14C105	105	14	SINGLE
ADC14DS105	105	14	DUAL
ADC14155	155	14	SINGLE
ADC14V155	155	14	SINGLE
ADC16V130	130	16	SINGLE
ADC16DV160	160	16	DUAL
ADC08D500	500	8	DUAL
ADC08500	500	8	SINGLE
ADC08D1000	1000	8	DUAL
ADC081000	1000	8	SINGLE
ADC08D1500	1500	8	DUAL
ADC081500	1500	8	SINGLE
ADC08(B)3000	3000	8	SINGLE
ADC08L060	60	8	SINGLE
ADC08060	60	8	SINGLE
ADC10DL065	65	10	DUAL
ADC10065	65	10	SINGLE
ADC10080	80	10	SINGLE
ADC08100	100	8	SINGLE
ADCS9888	170	8	SINGLE
ADC08(B)200	200	8	SINGLE
ADC11C125	125	11	SINGLE
ADC11C170	170	11	SINGLE

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REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	23

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6521SQ/NOPB	ACTIVE	WQFN	RTV	32	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L6521SQ	Samples
LMH6521SQE/NOPB	ACTIVE	WQFN	RTV	32	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L6521SQ	Samples
LMH6521SQX/NOPB	ACTIVE	WQFN	RTV	32	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L6521SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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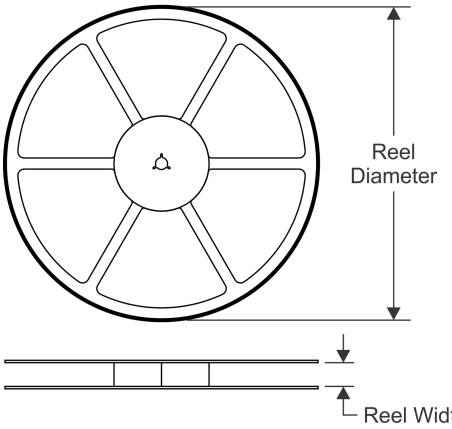
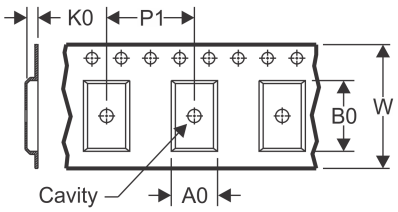
TAPE AND REEL INFORMATION

REEL DIMENSIONS

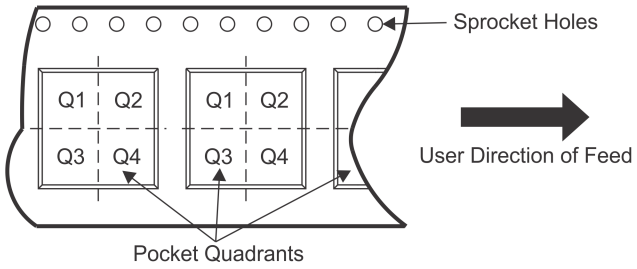


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

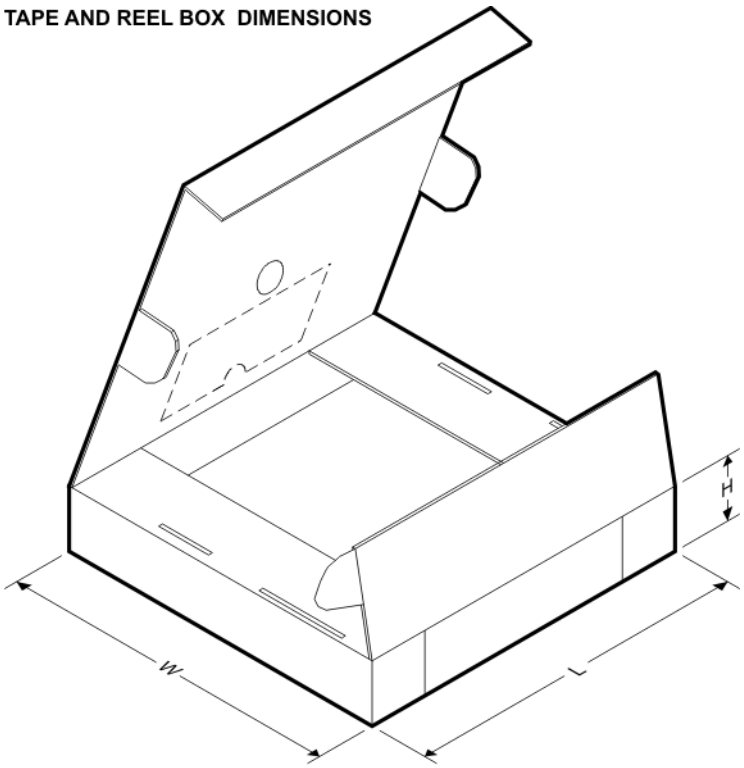
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6521SQ/NOPB	WQFN	RTV	32	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMH6521SQE/NOPB	WQFN	RTV	32	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

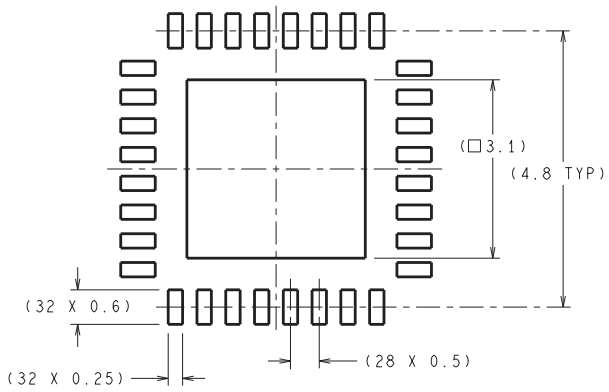
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

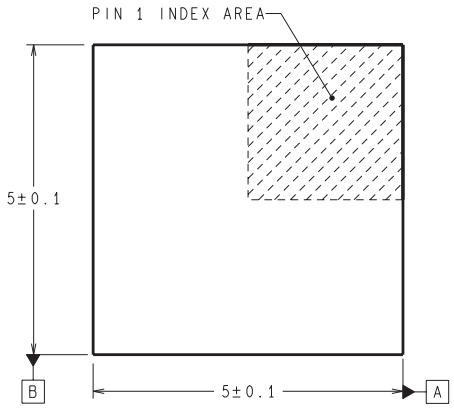
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6521SQ/NOPB	WQFN	RTV	32	1000	213.0	191.0	55.0
LMH6521SQE/NOPB	WQFN	RTV	32	250	213.0	191.0	55.0

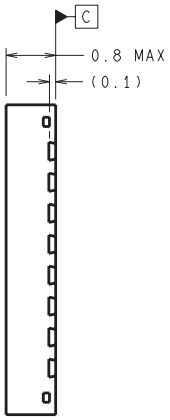
RTV0032A

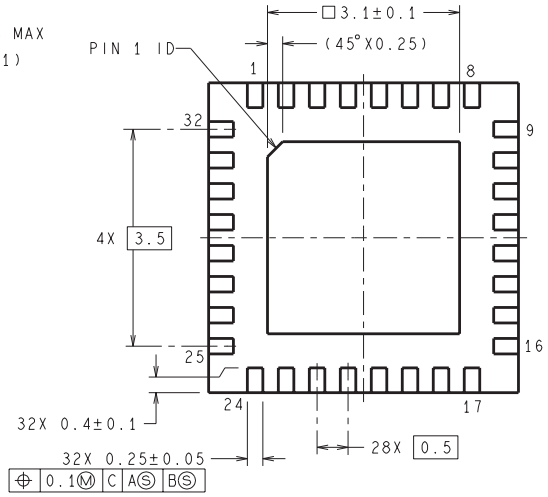


DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN







SQA32A (Rev B)

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