LIS331EB

iNEMO-A MEMS advanced 3D high performance accelerometer and signal processor

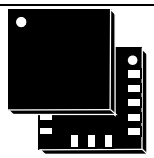
Data brief

Features

- Motions sensor:
  - Ultra low-power mode consumption down to 10 μA
  - $\pm 2g/\pm 4g/\pm 8g/\pm 16g$ selectable full scale
  - Data rate; 3.125 Hz to 1.6 KHz.
  - 16-bit data output
  - Embedded 2 State Machine
  - Embedded self-test
  - 10000 *g* high shock survivability
  - ECOPACK® RoHS and “Green” compliant
- Micro-core
  - Cortex-M0 core
  - 64 KB Flash Memory
  - 128 KB RAM memory
  - I^2C master port
  - I^2C slave port
  - SPI master/slave
  - 4 wires UART
  - 7 GPIO Interrupt capability
  - Low power features
  - 4 x 32-bit timers, Watchdog timer
  - Standard 4 wire JTAG and 2 wire SWD
  - 80 MHz / 32 KHz RC / external crystal oscillator

Applications

- Sensor hub
- Sensor fusion
- Gaming and virtual reality input devices
- LBS and augmented reality
- Enhanced navigation and motion tracking
- Vibration monitoring and compensation
- Pedometer
- Anti-tampering/antitheft system



LGA-16 (3x3x1 mm)

Description

The LIS331EB is an advanced low-power high performance smart sensor system in 3x3x1 mm LGA package, including a three-axis linear accelerometer (LIS3DSH) and Cortex-M0 core with 64 KB Flash, 128 KB RAM, RTC, timers, 2 I^2C (Master/Slave) and SPI (Master/Slave).

The device features ultra low-power operational modes that allow advanced power saving and smart sleep to wake-up functions.

The LIS331EB has dynamically user selectable full scales and it is capable of measuring accelerations with selectable output data rates up to 1.6 KHz. An embedded self-test capability allows the user to check the functioning of the sensor in the final application. A possible use of the LIS331EB is as a sensor hub.

The device can collect the inputs from accelerometers (embedded), gyroscopes, compasses, and pressure and other sensors through the master I^2C and elaborates/fuses together 9 or 10-axes (iNemo Engine software) to provide to the main app processor, for example, with the quaternions.

The LIS331EB is ECOPACK® RoHS and “Green” compliant.

Table 1. Device summary

Order codes	Temperature range [°C]	Package	Packaging
LIS331EB	-40 to +85	LGA-16	Tray
LIS331EBTR	-40 to +85	LGA-16	Tape and reel

Contents

1 General description

1.1 Accelerometer

The LIS331EB accelerometer is an ultra low-power high performance three-axis linear accelerometer belonging to the “nano” family with embedded state machine that can be programmed to implement autonomous applications.

The LIS331EB accelerometer has dynamically selectable full scales of ±2*g*/±4*g*/±6*g*/±8*g*/±16*g* and is capable of measuring accelerations with output data rates from 3.125 Hz to 1.6 KHz.

The self-test capability allows the user to check the functioning of the sensor in the final application.

The device can be configured to generate interrupt signals activated by user defined motion patterns.

The LIS331EB accelerometer has an integrated first in, first out (FIFO) buffer allowing the user to store data for host processor intervention reduction.

1.2 Microprocessor

The LIS331EB microprocessor is a single 32-bit processor capable of executing at a speed of 80 MHz down to 2.5 MHz with execution code from either Flash or SRAM with ECC. It integrates a low power RC 80 MHz oscillator with 192 Kilobytes of internal memory. An on-chip non volatile Flash memory allows processing.

The external host application processor, where the application resides, is interfaced with the LIS331EB microprocessor by means of a 2 wire serial port protocol which is based on a standard I^2C.

2 Block diagram and pin description

2.1 Block diagram

Figure 1. Block diagram accelerometer

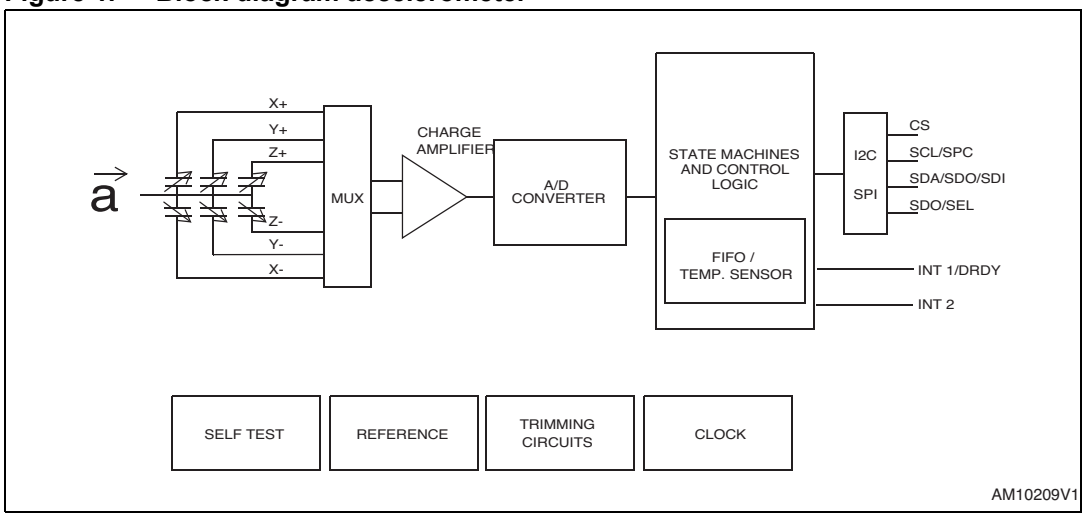
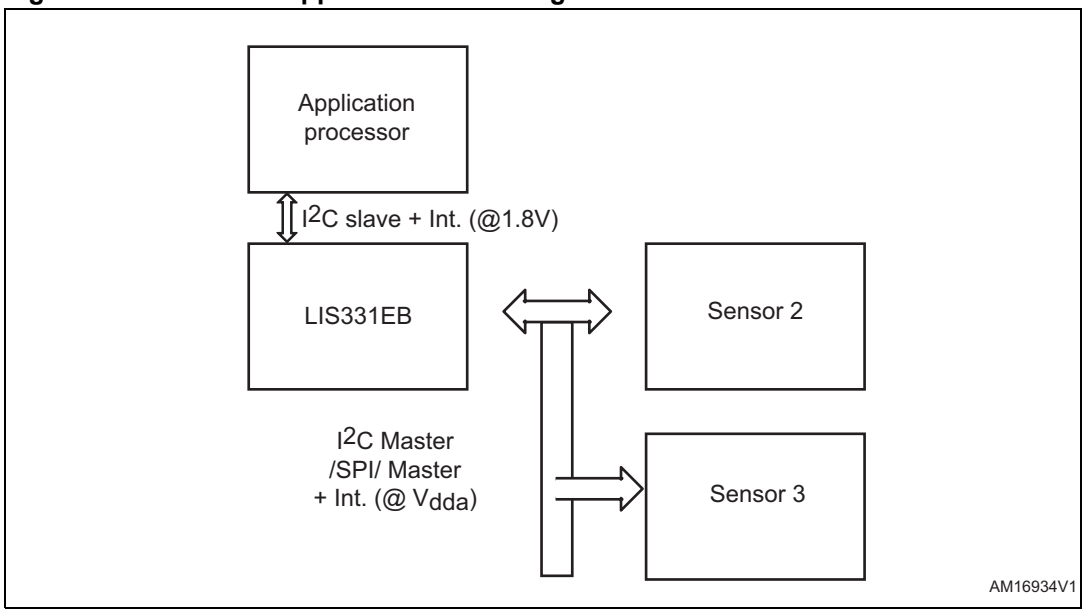


Figure 2. LIS331EB application block diagram



2.2 Pin description

Figure 3. Pin connection

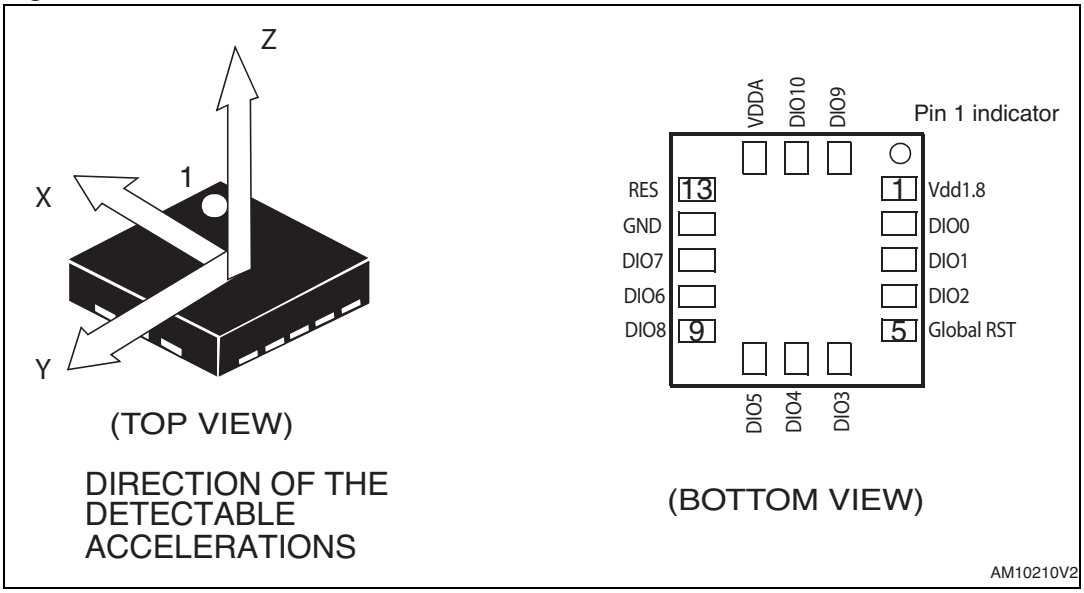


Table 2. Pin description

Pin#	Name	Function
1	Vdd1.8	Power supply for I/O pins 1.8 V
2	DIO0	GPIO0 / SW_TDIO / UART_CTS
3	DIO1	GPIO1 / SW_TCK / UART_RTS
4	DIO2	GPIO2 / I^2C serial clock (Slave SCL) / UART_TXD
5	Global RST	Reset
6	DIO3	GPIO3 / I^2C serial data (Slave SDA) / UART_RXD
7	DIO4	GPIO4
8	DIO5	GPIO5
9	DIO8	GPIO8 / I^2C serial data (Master SDA) / SPI_OUT
10	DIO6	GPIO6 / Divided clock 80 MHz / Clock 32 KHz
11	DIO7	GPIO7 / I^2C serial clock (Master SCL) / SPI_Clock
12	GND	0 V supply
13	Reserved	Connect to decoupling capacitor for 1.2 V digital regulator to GND
14	VDDA	Power supply for I/O pins 1.8 - 3.6 V
15	DIO10	GPIO10 / SPI_Input
16	DIO9	GPIO9 / SPI_CS

3 Accelerometer mechanical and electrical specifications

3.1 Mechanical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[a].

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
FS	Measurement range[2]	FS bit set to 000		±2.0		*g*
		FS bit set to 001		±4.0		*g*
		FS bit set to 010		±6.0		*g*
		FS bit set to 011		±8.0		*g*
		FS bit set to 100		±16.0		*g*
So	Sensitivity	FS bit set to 000		0.06		mg/digit
		FS bit set to 001		0.12		mg/digit
		FS bit set to 010		0.18		mg/digit
		FS bit set to 011		0.24		mg/digit
		FS bit set to 100		0.73		mg/digit
TCSo	Sensitivity change vs. temperature	FS bit set to 00		0.01		%/°C
TyOff	Typical zero-*g* level offset accuracy[3]	FS bit set to 00		±40		m*g*
TCOff	Zero-*g* level change vs. temperature	Max. delta from 25 °C		±0.5		m*g*/°C
An	Acceleration noise density	FS bit set to 00, normal mode, ODR = 100 Hz		150		u*g*/ sqrt(Hz)
ST	Self test positive difference[4]	± 2 *g* range, X,Y-axis ST2,ST1 = [01]		140		m*g*
		± 2 *g* range, Z-axis ST2,ST1 = [01]		590		
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Self-test output change" is defined as: $OUTPUT[mg]_{(CNTL5\ ST2,\ ST1\ bits=01)}$ - $OUTPUT[mg]_{(CNTL5\ ST2,\ ST1\ bits=00)}$

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

3.2 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[b].

Table 4. Electrical characteristics (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		1.71	2.5	3.6	V
Vdd_IO	I/O pins supply voltage(3)		1.71		Vdd+0.1	V
IddA	Current consumption in Active mode	1.6 KHz ODR		225		µA
		3.125 Hz ODR		11		µA
IddPdn	Current consumption in Power-down/Standby mode			2		µA
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication buses, in this condition the measurement chain is powered off.

3.3 Terminology

3.3.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined, e.g., by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations, this can be done easily by pointing the axis of interest towards the center of the earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, the actual sensitivity of the sensor is obtained. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.3.2 Zero-*g* level

The Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* in X axis and 0 *g* in Y axis, whereas the Z axis measures 1 *g*. The output is ideally in the center of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature" in *Table 3*. The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

b. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

3.4 Functionality

3.4.1 Self-test

Self-test allows the user to check the sensor functionality without moving it. The self-test function is off when the self-test bit (ST) is programmed to ‘0‘. When the self-test bit is programmed to ‘1’, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs exhibit a change in their DC levels which are related to the selected full-scale through the device sensitivity. When self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

3.5 Sensing element

A proprietary process is used to create a surface micro-machined accelerometer. The technology allows the construction of suspended silicon structures which are attached to the substrate at a few points called anchors, and are free to move in the direction of the sensed acceleration. To be compatible with traditional packaging techniques, a cap is placed on top of the sensing element to avoid blocking the moving parts during the moulding phase of the plastic encapsulation.

When an acceleration is applied to the sensor, the proof mass displaces from its nominal position, causing an imbalance in the capacitive half bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state, the nominal value of the capacitors are a few pF and when an acceleration is applied, and the maximum variation of the capacitive load is in the fF range.

3.6 IC interface

The complete measurement chain is made up of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage that is made available to the user through an analog-to-digital converter.

The acceleration data may be accessed through an I^2C/SPI interface, thereby making the device particularly suitable for direct interfacing with a microcontroller.

The LIS331EB features a Data-Ready signal (RDY) which indicates when a new set of measured acceleration data is available, simplifying data synchronization in the digital system that uses the device.

3.7 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-*g* level (TyOff).

The trimming values are stored inside the device in a non volatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the active operation. This allows use of the device without further calibration.

4 Accelerometer digital main blocks

4.1 State Machine

The LIS331EB embeds two State Machines capable of running a user-defined program.

The program is made up of a set of instructions that define the transition to successive states. Conditional branches are possible.

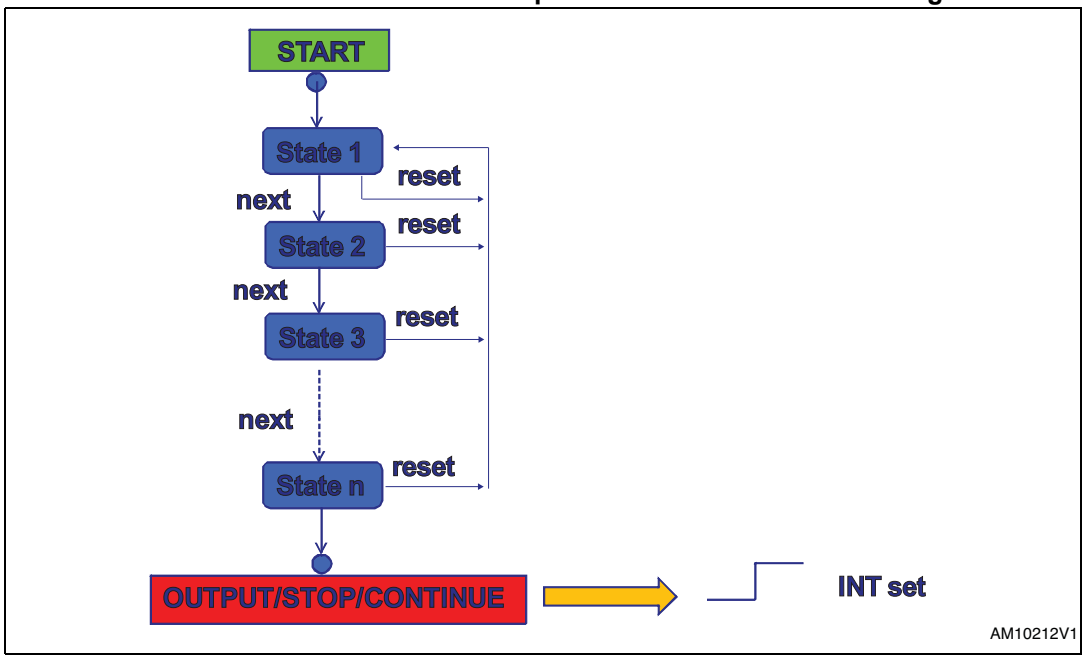
From each state (n) it is possible to transition to the next state (n+1) or to a reset state. The transition to reset point occurs when the “RESET condition” is true; Transition to the next step happens when the “NEXT condition” is true.

Interrupt is triggered when output/stop/continue state is reached.

Each State Machine allows implement gesture recognition in a flexible way, free-fall, wake-up, 4D/6D orientation, pulse counter and step recognition, click/double click, shake/double shake, face-up/face-down, and turn/double turn:

- Code and parameters are loaded by the host into dedicated memory areas for the state program
- State program with timing based on ODR or decimated time
- Possibility of conditional branches

Table 5. LIS331EB State Machines: sequence of state to execute an algorithm



4.2 FIFO

The LIS331EB embeds an acceleration data FIFO for each of the three output channels, X, Y, and Z. This allows consistent power savings for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work in four

different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits. Programmable Watermark level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the INT1/2 pin.

4.2.1 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. For each channel, only the first address is used. The remaining FIFO slots are empty.

4.2.2 FIFO mode

In FIFO mode, data from the X, Y, and Z channels are stored in the FIFO. A Watermark interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it is full. When full, the FIFO stops collecting data from the input channels.

4.2.3 Stream mode

In Stream mode, data from the X, Y, and Z measurement are stored in the FIFO. A Watermark interrupt can be enabled and set as in the FIFO mode. The FIFO continues filling until it is full. When full, the FIFO discards the older data as the new data arrive.

4.2.4 Stream-to-FIFO mode

In Stream-to_FIFO mode, data from the X, Y, and Z measurement are stored in the FIFO. A Watermark interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it is full. When full, the FIFO discards the older data as the new data arrive. Once a trigger event occurs, the FIFO starts operating in FIFO mode.

4.2.5 Retrieve data from FIFO

FIFO data is read through the OUT_X, OUT_Y and OUT_Z registers. When the FIFO is in Stream, Trigger or FIFO mode, a read operation to the OUT_X, OUT_Y or OUT_Z registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y, and Z data are placed in the OUT_X, OUT_Y and OUT_Z registers and both single read and read_burst operations can be used.

5 LIS331EB application hints

Figure 4. Application circuit with I²C sensors

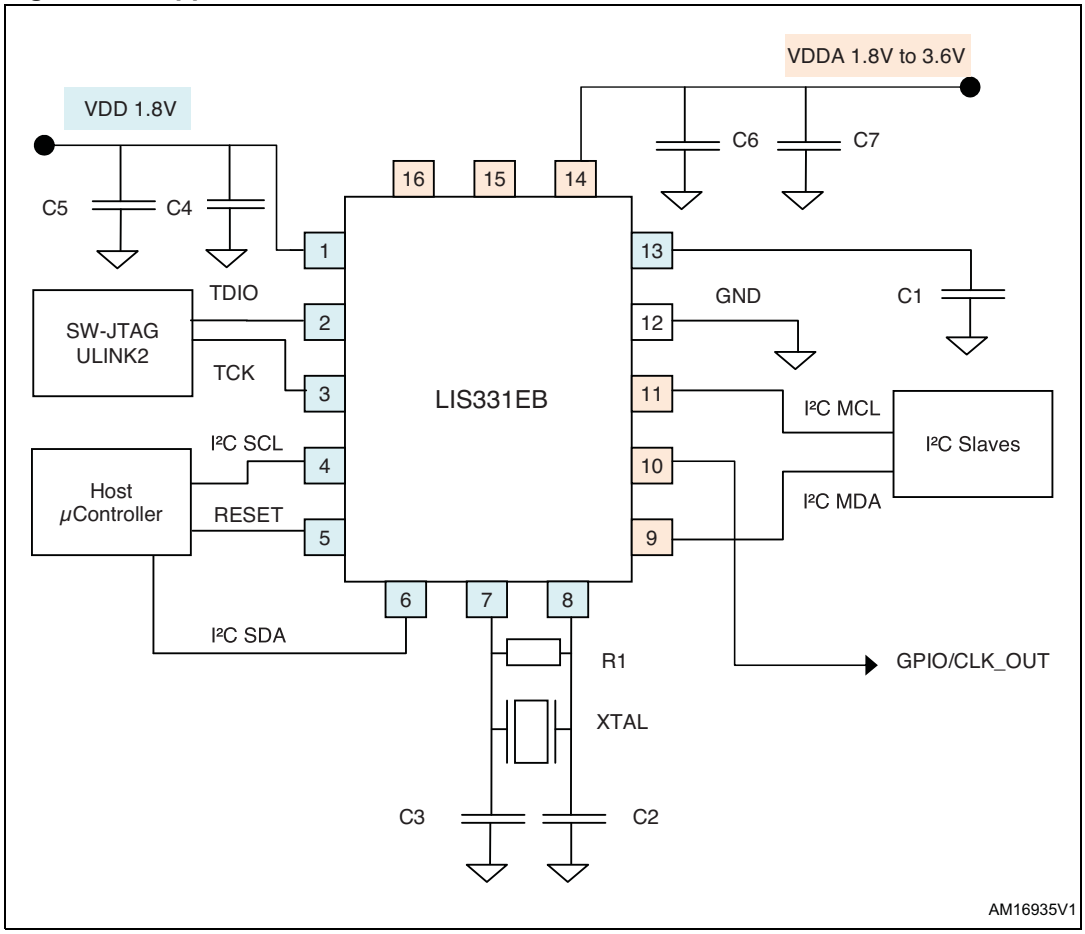
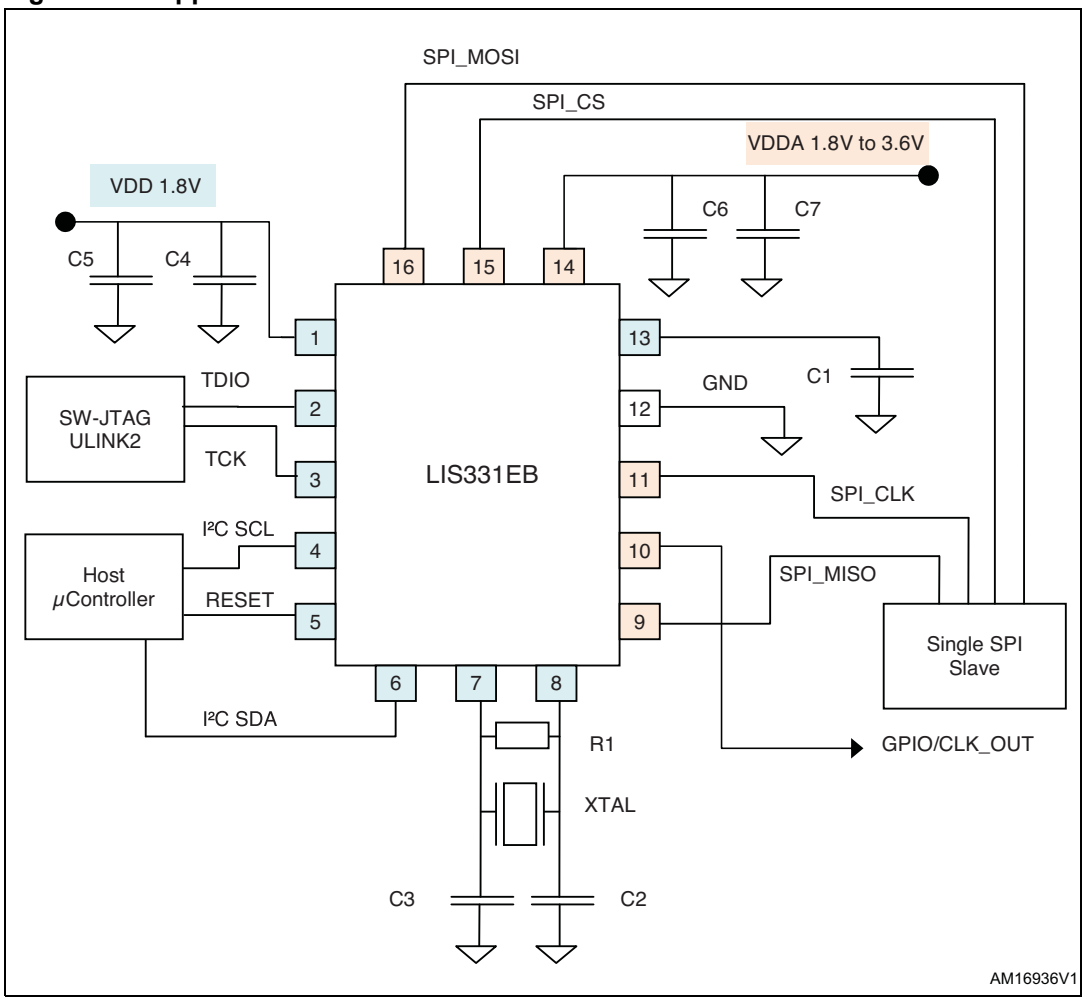


Table 6. External components list

Component	Description	Value
C1	Decoupling capacitor for 1.2 V digital regulator	1 µF
C2	32 KHz / 27 MHz crystal loading capacitor	15 pF
C3	32 KHz / 27 MHz crystal loading capacitor	15 pF
C4	Decoupling capacitor for 1.8 V digital regulator (LF)	1 µF
C5	Decoupling capacitor for 1.8 V digital regulator (HF)	100 nF
C6	Decoupling capacitor for 1.8 V – 3.6 V digital regulator (LF)	1 µF
C7	Decoupling capacitor for 1.8 V – 3.6 V digital regulator (HF)	100 nF
XTAL	32 KHz / 27 MHz crystal (optional)	TBD
R1	Oscillator feedback resistor	10 MOhms

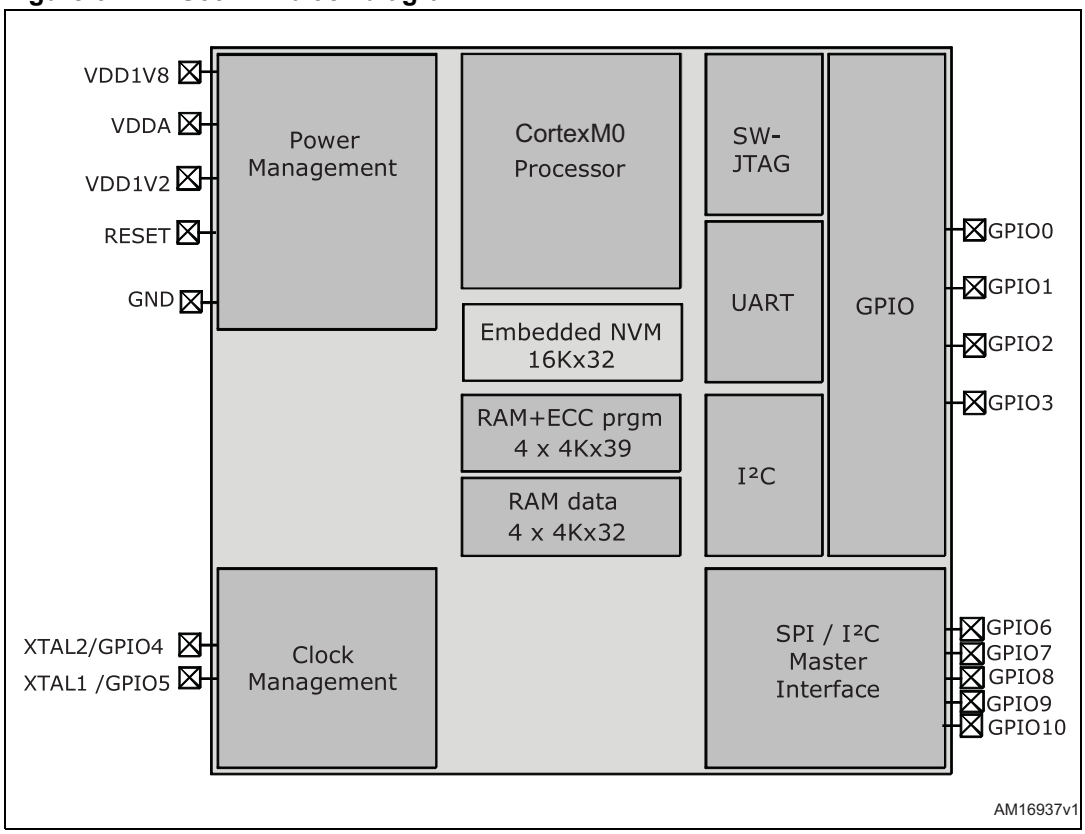
Figure 5. Application circuit with SPI sensors



6 Microprocessor block diagram

A block diagram of the LIS331EB is shown in *Figure 6*. In the following subsections, a short description of each module is given.

Figure 6. LIS331EB block diagram



6.1 Core, memory and peripherals

The LIS331EB contains an ARM Cortex-M0 microcontroller core that supports ultra low leakage state retention mode and almost instantaneously returning to fully active mode on critical events.

The memory subsystem consists of 64 KB Flash, 64 KB RAM with ECC for program and 64 KB RAM for data. Flash is used for the Cortex-M0 program as well as data logging.

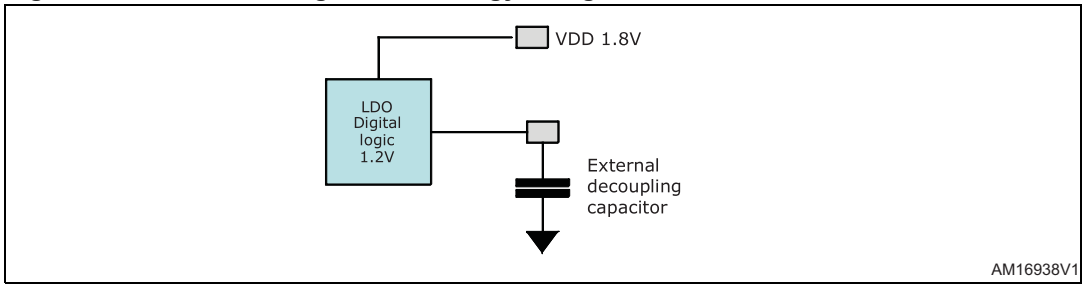
The IO controller handles the 11 general-purpose I/O pins, which can be configured to be controlled either by peripheral modules or by software. Each IO can be configured as an input, output and interrupt.

6.2 Power management

The LIS331EB integrates a low dropout voltage regulator (LDO) and is used to power the internal circuitry. The internal LDO supplies only the 1.2 V digital blocks, and requires a

decoupling capacitor for stable operation. *Figure 7* shows the simplified power management schemes using an LDO converter.

Figure 7. Power management strategy using LDO



6.3 Clock management

The microprocessor integrates a low speed (32 KHz) frequency oscillator (LSOSC), a high speed (80 MHz) frequency oscillator (HSOSC) and an external oscillator input.

The low frequency clock is used by real-time counters and watchdog timers and can be supplied either by a crystal oscillator that uses an external crystal and guarantee up to ±50 ppm frequency tolerance.

The primary high frequency clock is the internal 80 MHz RC oscillator.

7 Microprocessor operating modes

Several operating modes are defined for the LIS331EB:

- Reset mode
- Wait for interrupt mode (WFI)
- Active mode

In Reset mode the LIS331EB is in ultra low power consumption: all voltage regulators and clocks are un-powered. The LIS331EB enters Reset mode by asserting the external reset signal.

While in Wait for interrupt mode, the LIS331EB waits until an internal or external event occurs and then goes into Active mode. All internal blocks are powered, the clocks are free-running and almost all the logic is clock-gated.

To further reduce power in Wait for interrupt mode, the system clock can be fed by the external low frequency oscillator at a few KHz or MHz, while the high frequency 80 MHz oscillator can be powered down.

In Active mode the LIS331EB is fully operational: all interfaces, including SPI, I^2C, JTAG and UART, are active as are all internal power supplies together with the high speed frequency oscillator. The MCU core is also running.

Table 7 summarizes modes of operation and transition times.

Table 7. LIS331EB operating modes

State/mode	Digital LDO	SPI/I²C	LSOSC	HSOSC	XTAL OSC	CPU	Power	Response time-to active
Reset	OFF	OFF	OFF	OFF	OFF	OFF	1 μA	1 ms
WFI low power with external clock	ON	OFF	ON	OFF	ON	OFF (Clock gated)	700 μA	300 μs (ext. 32 KHz)
WFI high power	ON	ON	ON	ON	NA	OFF (Clock gated)	2 mA	50 ns
Active	ON	ON	ON	ON	NA	ON	9 mA(1)	NA

1. @ 80MHz.

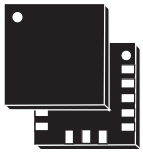
8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

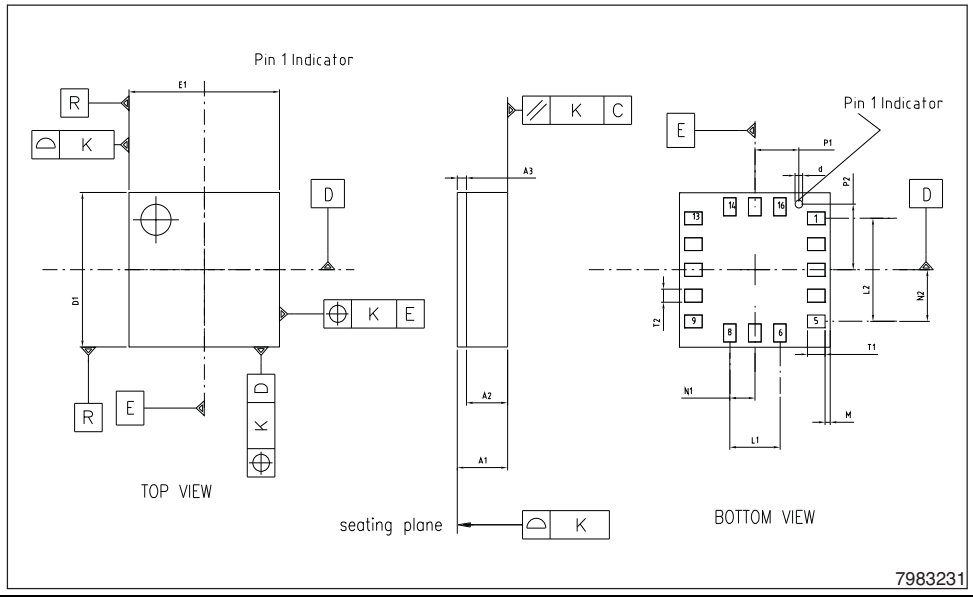
Figure 8. LGA-16: mechanical data and package dimensions

Ref.	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A1			1.000			0.0394
A2		0.785			0.0309	
A3		0.200			0.0079	
D1	2.850	3.000	3.150	0.1122	0.1181	0.1240
E1	2.850	3.000	3.150	0.1122	0.1181	0.1240
L1		1.000	1.060		0.0394	0.0417
L2		2.000	2.060		0.0787	0.0811
N1		0.500			0.0197	
N2		1.000			0.0394	
M	0.040	0.100	0.160	0.0016	0.0039	0.0063
P1		0.875			0.0344	
P2		1.275			0.0502	
T1	0.290	0.350	0.410	0.0114	0.0138	0.0161
T2	0.190	0.250	0.310	0.0075	0.0098	0.0122
d		0.150			0.0059	
k		0.050			0.0020	

Outline and mechanical data



LGA-16 (3x3x1.0mm)
Land Grid Array Package



9 Revision history

Table 8. Document revision history

Date	Revision	Changes
17-Jan-2013	1	Initial release.

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